



H6043 Manual

Electrical and mechanical specifications of the H6043 computer module

Title:	H6043 Manual
Subject:	Electrical and mechanical specifications of the H6043 computer module
Document number:	D0003
Version:	1.1
Last updated:	2/20/09

HECTRONIC AB
Box 3002
SE-750 03 UPPSALA
SWEDEN
TEL: +46 (0)18 660 700
FAX: +46 (0)18 660 701
EMAIL: info@hectronic.se
WEB: www.hectronic.se

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1 Document information

1.1 Abstract

This document is a hardware reference guide that provides basic information of the Hectronic H6043 embedded computer module. The manual is aimed for engineers who will integrate and/or design a carrier board for the Hectronic H6043 embedded computer module into their own products. The document includes memory maps, block diagram, board layout and interface descriptions as well as a U-Boot configuration guide etc.

1.2 Document revisions

Rev.	Date	Sign	Description
1.0	2008-01-31	Daniel Skaborn	Initial release.
1.1	2008-03-25	Jonas Antoni	Reorganized the manual to make it similar to the H6042 manual.

Table 1: Document revisions.

1.3 References

No.	Description
[1]	H4091 Manual
[2]	http://www.atmel.com/dyn/resources/prod_documents/doc1768.pdf

Table 2: Document references.

2 Safety Instructions



Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operation life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep the board in its ESD shielding bag until you are ready to install it.
- Before touching the board, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the device only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold the device only by its edges and mounting hardware. Avoid touching components and connector pins.
- Please assure ESD compliant handling of the board when unpacking and connecting peripherals.
- Never connect or disconnect external peripherals with power on.

- Please study all the information in this document carefully before applying power to the system.
- For further information on ESD, visit www.esda.org

3 Product overview

The H6043 is designed to provide embedded solution easily adopted to a specific specialized application. The module is based on an ARM9 CPU architecture, the module includes Li-Ion battery charge controller. H6043 implements a range of standard interfaces, such as 10/100 Mbit/s Ethernet, Serial ports, USB host, USB device, SPI, I2C. These features together with the very small outline, targets this board to a range of handheld and embedded products.

H6043 may run Linux or WindowsCE.

3.1 Module Layout

Key components and connector functions.

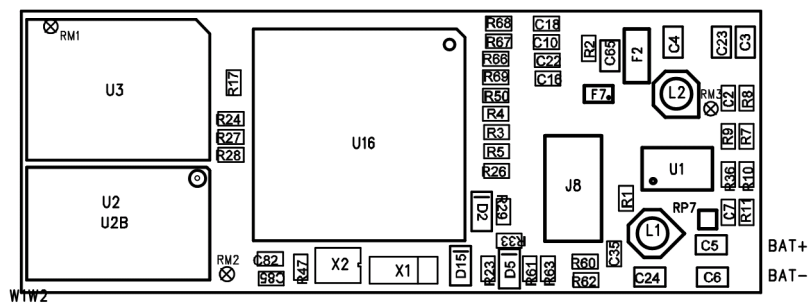


Figure 1: H6043 top side view

J8	dbgport (PA30, PA31), BMS, JTAG
U16	CPU
U3	P30 FLASH
U1	Core power regulators, and charge regulator
U2	SDRAM
BAT+ BAT-	Battery connector.

3.2 Models and options

Model	Description
H6043	Computer module, ARM-based cpu board with 16MB flash and 32 MB SDRAM.

Table 3: H6043 Models.

3.3 Carrier boards

Model	Description
H4091	Carrierboard

Table 4: Carrier boards.

4 Product specifications

4.1 Mechanical

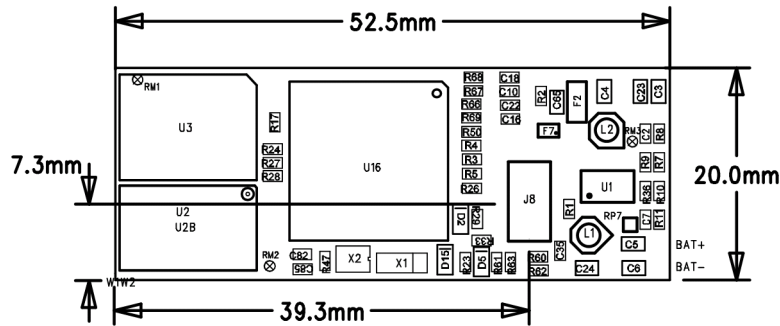


Figure 2: Mechanical drawing, top side view

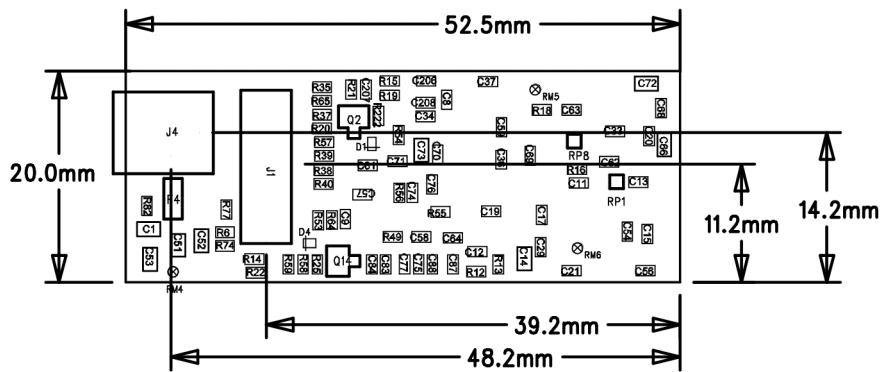


Figure 3: Mechanical drawing, bottom side view

4.1.1 Carrier board mounting

The board-to-board connectors do not give enough mechanical support. The module should be given sufficient mechanical support from surrounding mechanics.

4.1.2 Component heights

Board-to-board stacking height is 4.0 mm. Max component height on the CPU board is 4.0 mm on bottom side, and 1.1 mm on top side (excluding the height of connector J8).

Note that the height of connector J1 on the bottom side will affect the layout of a carrier board due to the height of the component.

No hot components should be placed below or above the CPU board.

4.2 Electrical specification

4.2.1 Power consumption

The power consumption is dependent of the system configuration. Running software Processor load and speed mode, memory and attached devices.

Module	Max dissipation at 3.7V (battery)	Typical dissipation at 3.7V (battery)	Max dissipation at 5V	Typical dissipation at 5V	Unit
H6043	205	145	155	100	mA

Table 5: Theoretical power consumption.

The dissipation numbers are theoretical calculated values.

4.2.2 Power supply requirements

The H6043 requires the power supply sources to be within voltage ranges to work properly.

Supply	Min	Max	Unit
VCC 3.7V battery	3.5	4.1	V
VCC 5.0V	see note		V

Table 6: Power supply requirements.

Note that use on USB host interface requires the 5V output to USB devices (check USB 2.0 specification for details).

4.3 Thermal

In operation areas where the board is surrounded by air there is no need for nor active cooling or passive heat sink.

5 Board description

5.1 Block diagram

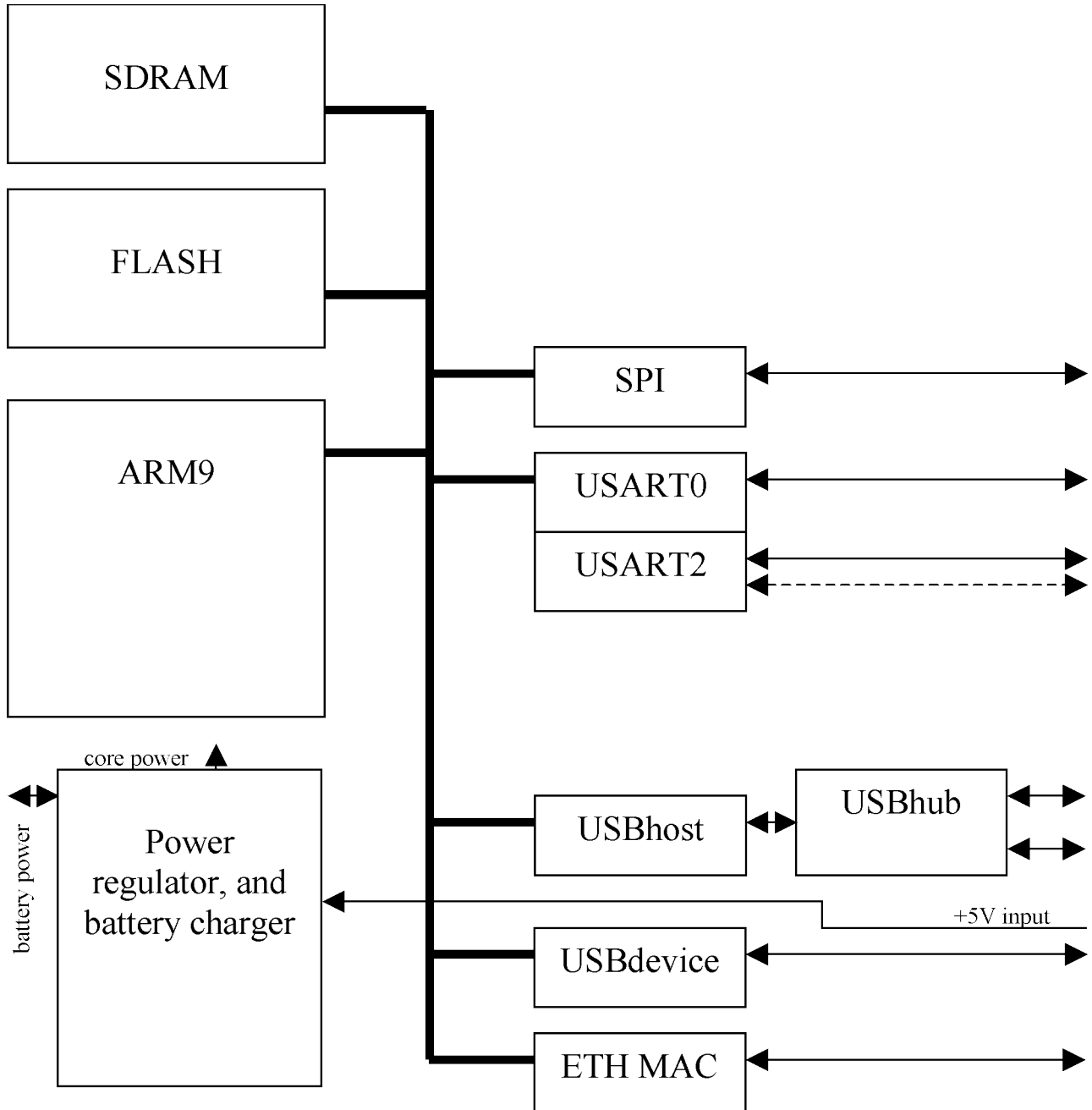


Figure 4: H6043 block diagram

5.2 ARM9

The CPU on the H6043 is an Atmel AT91RM9200. The processor is an ARM920T based CPU running at 180MHz, 200MIPS.

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5.3 SDRAM

256Mbit, (32Mbyte) mobile SDRAM.

5.4 FLASH

128Mbit, (16Mbyte) Intel strata P30 embedded flash. There is an option to mount 256 Mbit (32 Mbyte) flash.

5.5 SPI - Serial Peripheral Interface

The interface supports communication with serial external devices. Four chip selects. External decoder may be implemented in FPGA.

SPI may be used to communicate with serial memories, such as dataFlash and 3-wire EEPROMs, and serial peripherals such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors External co-processors.

5.6 I2C

Two-wire Interface, aka I2C, compatibility with standard two-wire serial memory is supported.

5.7 USART0

The USARTs has Programmable Baud Rate Generator. 5- to 9-bit full-duplex synchronous or asynchronous serial communications 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode Parity generation and error detection Framing error detection, overrun error detection.

USART0 implements RX, TX.

5.8 USART2

Debug port RX, TX.

5.9 USB host and USB hub

Compliance with Open HCI Rev 1.0 specification. Compliance with USB V2.0 Full-speed and Low-speed specification. Supports both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices. The USB root hub integrates two downstream USB ports.

5.10 USB device

USB V2.0 full-speed compliant, 12 Mbits per second. Embedded USB V2.0 full-speed transceiver. Embedded dual-port RAM for endpoints.

Suspend/Resume logic Ping-pong mode (two memory banks) for isochronous and bulk endpoints. Six general-purpose endpoints;

Endpoint 0, Endpoint 3: 8 bytes, no ping-pong mode

Endpoint 1, Endpoint 2: 64 bytes, ping-pong mode

Endpoint 4, Endpoint 5: 256 bytes, ping-pong mode

5.11 ETH MAC, Ethernet Medium Access Control, 10/100 controller

Compatibility with IEEE Standard 802.3

10 and 100Mbps per second data throughput capability. Full- and half-duplex operation. MII or RMII interface to the physical layer. Register interface to address, status and control registers. DMA interface, operating as a master on the Memory Controller. Interrupt generation to signal receive and transmit completion. 28-byte transmit and 28-byte receive FIFOs. Automatic pad and CRC generation on transmitted frames. Address checking logic may recognize four 48-bit addresses. Supports promiscuous mode where all valid frames are copied to memory. Supports physical layer management through MDIO interface.

5.12 ETH PHY, Ethernet Physical layer interface

H6043 is not equipped with a Ethernet PHY. Though are the dedicated GPIOs interfacing the phy routed to the carrier board connector.

5.13 LEDES

The H6043 has three status LEDs which many be used for any purpose. These LEDs are connected to ARM PB0, ARM PB1 and ARM PB2 GPIO pins.

6 Quality and environmental data

6.1 Required environmental conditions

Temperature ambient, operating	-40 to +80 °C
Temperature ambient, storage	-40 to +80 °C

Table 7: Environmental contidions.

6.2 EMC compliance

When correctly installed in a suitable chassis with recommended filtering on carrier-board as described in the design guidelines, the H6043 is designed to meet the following EMC regulations:

EN50081-1 Generic emission standard for residential commercial and light industry use.

CISPR25 RF-disturbances for vehicles (e-type approval).

6.3 Saftey compliance

Depending on carrier board design, and mechanic casing.

6.4 Industry standard compliances

The H6043 implements the following industry standards. To fulfil the standards some filtering / drivers is needed on the carrier board:

Standard	Description	Reference
----------	-------------	-----------

USB2.0	Universal Serial Bus rev 2.0	http://www.usb.org
IEEE 802.3i ¹	10baseT Ethernet 10 twisted pair	http://www.ieee.org
IEEE 802.3u ¹	Fast Ethernet100Base-Tx	www.ieee.org
I2C	Inter-Integrated Circuit bus	Phillips semiconductors
SPI	Serial Peripheral Interface BUS	Motorola
EIA RS232 / RS485 ²	Serial port standard	EIA
IEEE 1149.1	JTAG Boundary Scan (ARM CPU)	IEEE

Table 8: Industry standard compliances

¹ Requires Ethernet PHY and magnetics on carrier board.

² The linedriver circuitry is to be placed on the carrier board. H6043 hosts the UART.

6.5 Quality ensures and milieu influences

RoHS compliant

ISO9001

ISO14001

6.5.1 WEEE 2002/96/EC

The H6043 is intended to be included in a product. The responsibility when it comes to recycling and registering the end product with the correct authorities lies at the producer of the end product.

7 Design guide lines

This section contains some hints when designing a carrier board for the H6043.

7.1 Buses

7.1.1 USB

In [2], chapter 35 the USB interface is described.

7.1.2 Ethernet

The ethernet signals from the H6043 must be completed with an ethernet PHY, magnetics and a suitable connector.

In [2], chapter 36 the ethernet interface is described.

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7.1.3 I2C

The I²C bus is available at [J1](#) pins marked with TWCK and TWD. TWCK is the I²C clock, and TWD is the I²C data.

In [2], chapter 29 the I² interface is described.

7.1.4 SPI

In [2], chapter 28 the SPI interface is described.

7.2 Devices

7.2.1 ARM PA31

The GPIO PA31 is the BMS (boot mode select) which is sampled by the AT91RM9200 at boot time, if the PA31 is asserted high the AT91RM9200 will go into a "download firmware" state. To ensure normal operation, leave this pin in high impedance state during boot up.

7.2.2 GPIO

Many of the I/O pins on the AT91RM9200 CPU has multiple functions, the connector table for [J1](#) (pins marked with class "alog" or "eth") shows all functions that are available on the H6043.

7.3 Power supply

7.3.1 +3.7 V battery

The +3.7 V lilon battery must be able to provide as much current as specified in the [power consumption](#) table.

7.3.2 +5 V

The +5 V power supply must be able to provide as much current as specified in the [power consumption](#) table.

Appendix A Firmware reference

A.1 Bootloader, U-boot

U-boot is a bootloader supporting boot from flash, USBmemory, Ethernet and serialport. The purpose of the bootloader is to bring the target board to a state where an operating system can be loaded and executed. This means that U-boot does some basic hardware initializations (PLL:s, SDRAM, UART:s, network devices, etc).

H6043 is shipped with U-boot installed in the flash memory.

A.2 Bootstrap

The Bootstrap is the procedure to program the bootloader to the H6043.

Two versions of U-boot are actually needed. One version doing the initialisations described in [2], and another version not doing these initialisations. Let's call the latter u-boot-h6043-latest-no_hwinit.bin and the former (more complete) u-boot-h6043-latest.bin.

The Bootstrap mode is entered when the BMS-pin is active, at bootstrap the communication is done by the debug serial port.

The steps involved to do the bootstrapping are:

1. Upload loader.bin to the target board's SRAM using sx-at91. This initiates the target board's SDRAM memory and initiates another xmodem receive sequence that places the next transfer in SDRAM.
2. Upload u-boot-h6043-latest-no_hwinit.bin into SDRAM. Note that this is NOT the u-boot that we want to put into flash memory. Since loader.bin did the necessary initialisation of the hardware, u-boot must not do that.
3. Start a terminal emulator on the connected serial port.
4. Use the command line interface to download u-boot-h6043-latest.bin to SDRAM.
5. Write u-boot-h6043-latest.bin to flash memory.

A.3 U-boot Setup configuration, default setup, update

Please refer to U-boot documentation, and Hectronic SW application notes and getting started guides to get details about these subjects.

There are more information about U-boot in the Helix documentation.

Appendix B Connectors and pin outs

B.1 Connector placements

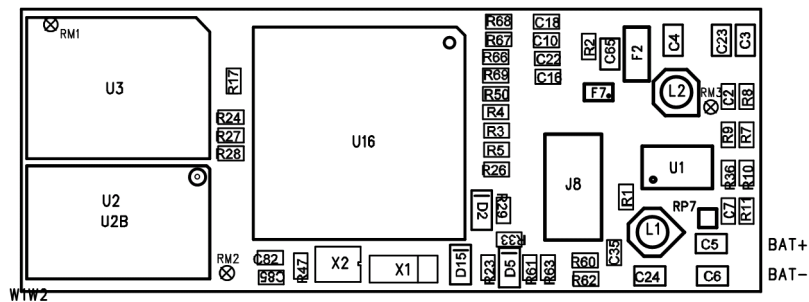


Figure 5: H6043 connector placement drawing, top side view

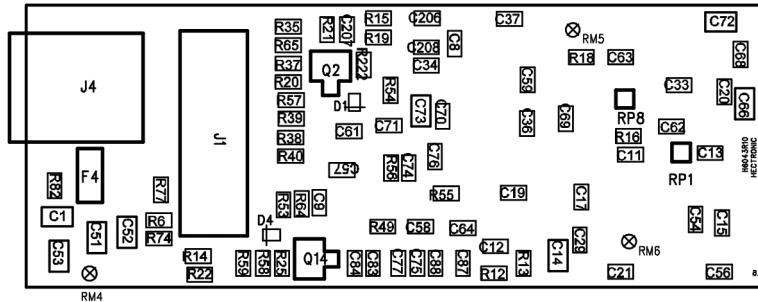


Figure 6: H6043 connector placement drawing, bottom side view

B.2 J4 USB B mini socket (device)

USB type B socket

pin#	signal	class
1	VCC +5V input	powi
2	D-	usb
3	D+	usb
4	NC (id)	
5	GND	powi

Table 9: J4 pinning.

B.3 J2 alternative power supply battery connector

2.54mm jumper header

pin#	signal	class
1	GND	pow
2	BAT +	bat
3	KILL-	bat
4	GND	pow

Table 10: Battery connector pinning.

B.4 J8 Debug / programming header (incl BMS)

Connector: CVILUX CBRB020PC2FP1R0

pin#	signal	class
1	VCC +3.3V	powo
2	ARM JTAG TCK	alog
3	VCC +3.3V	powo
4	ARM JTAG TDI	alog
5	BAT+	bat
6	ARM JTAG TDO	alog
7	BAT+	bat

8	ARM JTAG TMS	alog
9	ARM PC13	alog
10	PWR GOOD	powg
11	+5V IN	powi
12	GND	powi
13	GND	powi
14	GND	powi
15	GND	powi
16	BMS	bms
17	VCC 1.8V	
18	ARM PA31/dbg TX	alog
19	VCC 1.8V	
20	ARM PA30/dbg RX	alog

Table 11: J8 pinning.

B.5 J1 Carrier board header

Connector: CVILUX CBRB040SC2FP1R0

pin#	signal	class
1	GND	powi
2	GND	powi
3	USB0 D+	usb
4	VCC +3.3V	powo
5	USB0 D-	usb
6	USB device D+	usb
7	USB1 D+	usb
8	USB device D-	usb
9	USB1 D-	usb
10	ARM PA15/EMDC	eth
11	ARM PA7/REFCK	eth
12	ARM PA16/EMDIO	eth
13	ARM PA10/ETX1	eth
14	ARM PC4/IRQERX1	eth
15	ARM PA9/ETX0	eth
16	ARM PA18/UART0 RXD	alog
17	ARM PA8/ETXEN	eth
18	ARM PA5/SPI NPC2	alog
19	ARM PA13/ERX1	eth
20	ARM PA4/SPI NPC1	alog
21	ARM PA12/ERX0	eth
22	ARM PA2/SPI CLK	alog

23	ARM PB8	alog
24	ARM PA0/SPI MISO	alog
25	ARM PB9	alog
26	ARM PA1/SPI MOSI	alog
27	ARM PB10	alog
28	ARM PB13	alog
29	ARM PB11	alog
30	ARM PA26/TWCK	alog
31	ARM PA17/UART0 TXD	alog
32	ARM PA25/TWD	alog
33	PWR GOOD	powg
34	+5V in	powi
35	ARM PA11/ECRSDV	eth
36	+5V in	powi
37	ARM PA14/ERXER	eth
38	BAT+	bat
39	GND	powi
40	BAT+	bat

Table 12: J1 pinning.

Appendix C Signal characteristics

Here follows descriptions of the different signal classes on the board. Each signal in the pin signal listings in chapter 2 have a class tag.

C.1 bms - boot mode select

The boot mode select is a configuration signal samples at startup. The pin is shared with a debug serial port on the CPU. To enter boot strap mode this signal is to be pulled up to 3.3V. In practice, connect a 8k2 resistor over pin1 and pin2 at the J7 connector.

C.2 powi - Power input line

This is a power input supply connection.

C.3 powo - Power output line

This is a power output supply connection.

The H6043 can supply a carrier board with 100 mA @ 3.3 V.

The 1.8 V available on the connectors may not be used for powering carrier boards.

C.4 eth - Ethernet data signal

The Ethernet signals are ARM I/O signals which must be completed with an ethernet PHY circuit, magnetics and a suitable connector.

These signals are also possible to use as GPIO, but that will inhibit the use of the ethernet interface.



Maximum voltage that may be applied to these pins are 3.6V.

C.5 alog - ARM CPU logic level signal

ARM CPU logic level signal. Pins has a programmable pull-up resistor of 15kOhm. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that must be enabled as peripherals at reset. Signals is 3.3V logic level.

The full electric specification of the GPIO pins may be found in [2].



Maximum voltage that may be applied to these pins are 3.6V.

C.6 powg - Power good

Output signal from the H6043 power converter. This signal is asserted high when the 3.3 V and 1.8V are stable.

C.7 usb - USB data signal

The USB signals are differential pairs. Length matching, maximum length and differential impedance is critical design parameters. The pairs should be common mode filtered before cable connector to avoid conductive EMC problems.

C.8 bat - Battery

Battery positive pole. This supplies the H6043 with power from a battery. The H6043 also contains a charging circuit for the battery.

The battery must be a Lilon 3.7 V and accept a charging voltage of 4.2 V.

Appendix D Interrupt, device and address assignments

D.1 Memory map

Address [hex]	Device	Size [bytes]
0x0000 0000 - 0x000F FFFF	Boot memory	1M
0x0010 0000 - 0x001F FFFF	ROM	1M
0x0020 0000 - 0x002F FFFF	SRAM	1M
0x0030 0000 - 0x003F FFFF	USB Host	1M

	Undefined	
0x1000 0000 - 0x1FFF FFFF	EBI Chip select 0 / BFC	256M
0x2000 0000 - 0x2FFF FFFF	EBI Chip select 1 / SDRAMC	256M
0x3000 0000 - 0x3FFF FFFF	EBI Chip select 2	256M
0x4000 0000 - 0x4FFF FFFF	EBI Chip select 3 / NAND Flash Logic	256M
0x5000 0000 - 0x5FFF FFFF	EBI Chip select 4 / CF Logic	256M
0x6000 0000 - 0x6FFF FFFF	EBI Chip select 5 / CF Logic	256M
0x7000 0000 - 0x7FFF FFFF	EBI Chip select 6 / CF Logic	256M
0x8000 0000 - 0x8FFF FFFF	EBI Chip select 7 / CF Logic	256M
	Undefined	
0xF000 0000 - 0xFFFF 9FFF	Reserved	
0xFFFFA 0000 - 0xFFFFA 3FFF	TCO, TC1, TC2	16K
0xFFFFA 4000 - 0xFFFFA 7FFF	TC3, Tc4, TC5	16K
0xFFFFA 8000 - 0xFFFFA FFFF	Reserved	16K
0xFFFFB 0000 - 0xFFFFB 3FFF	UDP	16K
0xFFFFB 4000 - 0xFFFFB 7FFF	MCI	16K
0xFFFFB 8000 - 0xFFFFB BFFF	TWI	16K
0xFFFFB C000 - 0xFFFFB FFFF	EMAC	16K
0xFFFFC 0000 - 0xFFFFC 3FFF	USART0	16K
0xFFFFC 4000 - 0xFFFFC 7FFF	USART1	16K
0xFFFFC 8000 - 0xFFFFC BFFF	USART2	16K
0xFFFFC C000 - 0xFFFFC FFFF	USART3	16K
0xFFFFD 0000 - 0xFFFFD 3FFF	SSC0	16K
0xFFFFD 4000 - 0xFFFFD 7FFF	SSC1	16K
0xFFFFD 8000 - 0xFFFFD BFFF	SSC2	16K
0xFFFFD C000 - 0xFFFFD FFFF	Reserved	
0xFFFFE 0000 - 0xFFFFE 3FFF	SPI	16K
0xFFFFE 4000 - 0xFFFFE F0FF	Reserved	
0xFFFFF F100 - 0xFFFFF F1FF	AIC	512
0xFFFFF F200 - 0xFFFFF F3FF	DBGU	512
0xFFFFF F400 - 0xFFFFF F5FF	PIOA	512
0xFFFFF F600 - 0xFFFFF F7FF	PIOB	512
0xFFFFF F800 - 0xFFFFF F9FF	PIOC	512
0xFFFFF FA00 - 0xFFFFF FBFF	PIOD	512
0xFFFFF FC00 - 0xFFFFF FCFF	PMC	256
0xFFFFF FD00 - 0xFFFFF FDFF	ST	256
0xFFFFF FE00 - 0xFFFFF FEFF	RTC	256
0xFFFFF FF00 - 0xFFFFF FFFF	MC	256

Table 13: Memory map.

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D.2 Interrupt allocation

Appendix E Notational conventions and acronyms used

E.1 Notational conventions

All number are decimal unless otherwise stated.

Bit 0 is the low-order bit.

If a bit is set to 1, the associated description is true unless otherwise stated.

E.2 Acronyms

ESD - Electro Static Discharge

EMC - ElectroMagnetic Compability

RMA - Return Material Authorization

PCI - Peripheral Component Interconnect

USB - Universal Serial Bus

RTC - Real Time Clock

SPI - Serial Peripheral Interface

USART - Universal Synchronous/Asynchronous Receiver/Transmitter

FPGA - Field Programmable Gate Array

PHY - Ethernet physical layer

MAC - Ethernet medium access control

UTP - Unshielded Twisted Pair

MDIO - Management Data Input/Output (IEEE 802.3)

MII - Media Independent Interface

RMI - Reduce Media Independent Interface

FIFO - First in First out data buffer

CRC - Cyclic Redundancy Check

ADC - Analogue to Digital converter

DAC - Digital to Analogue converter

LCD - Liquid Crystal Display

CAN - Controller Area Network (field-bus often used in vehicles)

SDRAM - Synchronous Dynamic Random Access Memory

Appendix F Product care and maintenance

The H6043 is a "naked board" aim to be embedded in a product and casing. Therefore the board is sensitive for ESD and should be handled in ESD safe environment. At least utilize a wrist-strap when handled, but preferably handle the board in a ESD-safe lab or production area.

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When the board is mounted on a carrier board make shore the boards signalground is at the same potential. This may be reach safely by connecting the signal ground of the boards to a common GND, with a series resistor.

Always remember to power off the system when assembling and disassembling.

Appendix G RMA - Return Material Authorization

In case of a malfunction unit, the following RMA procedure is to be used.

Contact Hectronic support department at support@hectronic.se. The support department will guide you through the RMA process.

Appendix H Hectronic ARM board family summary

Article	Description
H6042	ARM board with a Spartan FPGA as a companion chip
H4090	Reference carrier for H6042
H6043	Very small ARM board
H4091A	Carrier board for H6043, equipped with Ethernet PHY and USB and a +5V step-up converter
H4091B	Debug connector board for H6043.
H4091C	Button board for connection to H4091A
H4091D	RFID board, for connection to H4091A

Table 14: Hectronic ARM products.