HECTRONIC

H6042 Manual

Electrical and mechanical specifications of the H6042 computer module

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1 Document information

1.1 Abstract

This document is a hardware reference guide that provides basic information of the Hectronic H6042 embedded computer module. The manual is aimed for engineers who will integrate and/or design a carrier board for the Hectronic H6042 embedded computer module into their own products. The document includes memory maps, block diagram, board layout and interface descriptions as well as a U-Boot configuration guide etc.

1.2 Document revisions

Rev.	Date	Sign	Description
1.0	2007-04-03	Daniel Skaborn	Initial release.
1.1	2007-04-04	Daniel Skaborn / Kristoffer Eriksson	Non connected pins clearly marked. Stacking height added. Bus design consideration added.
1.2	2007-04-10	Daniel Skaborn	Added Artno for main ICs. Added IO list for FPGAs. Enlarged pictures. Power estimation.
1.3	2007-08-02	Daniel Skaborn	Added H6042 component height information. Added H4090 reference carrier information.
1.4	2008-02-02	Erik Jansson	Moved H4090 information to separate manual.
1.5	2008-03-20	Jonas Antoni	Proof reading and correction.
1.6	2008-05-12	Jonas Antoni	Added chapter about FPGA interface.

Table 1: Document revisions.

1.3 References

No.	Description
[1]	H4090 Manual
[2]	http://www.atmel.com/dyn/resources/prod_documents/doc1768.pdf
[3]	http://www.xilinx.com/ise/logic_design_prod/webpack.htm

Table 2: Document references.

2 Safety Instructions

Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operation life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep the board in its ESD shielding bag until you are ready to install it.

- Before touching the board, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the device only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold the device only by its edges and mounting hardware. Avoid touching components and connector pins.
- Please assure ESD compliant handling of the board when unpacking and connecting peripherals.
- Never connect or disconnect external peripherals with power on.
- Please study all the information in this document carefully before applying power to the system.
- For further information on ESD, visit www.esda.org.

3 Product overview

The H6042 is designed to provide embedded solution easily adopted to a specific specialized application. The module is based on a ARM9 CPU architecture and is equipped with an FPGA. The FPGA is not pre-configured in any way and is fully dedicated to perform some application-specific task. This feature targets the this board to a very wide range of applications with some demands that is typically implemental by an FPGA.

The product implements a range of standard interfaces, such as 10/100 Mbit/s Ethernet, Serial ports, USB host, USB device, SPI, I2C.

H6042 may run Linux, WindowsCE or a real-time operating system. Contact Hectronic AB for information on BSP availability.

3.1 Module layout

Key components and connector functions.

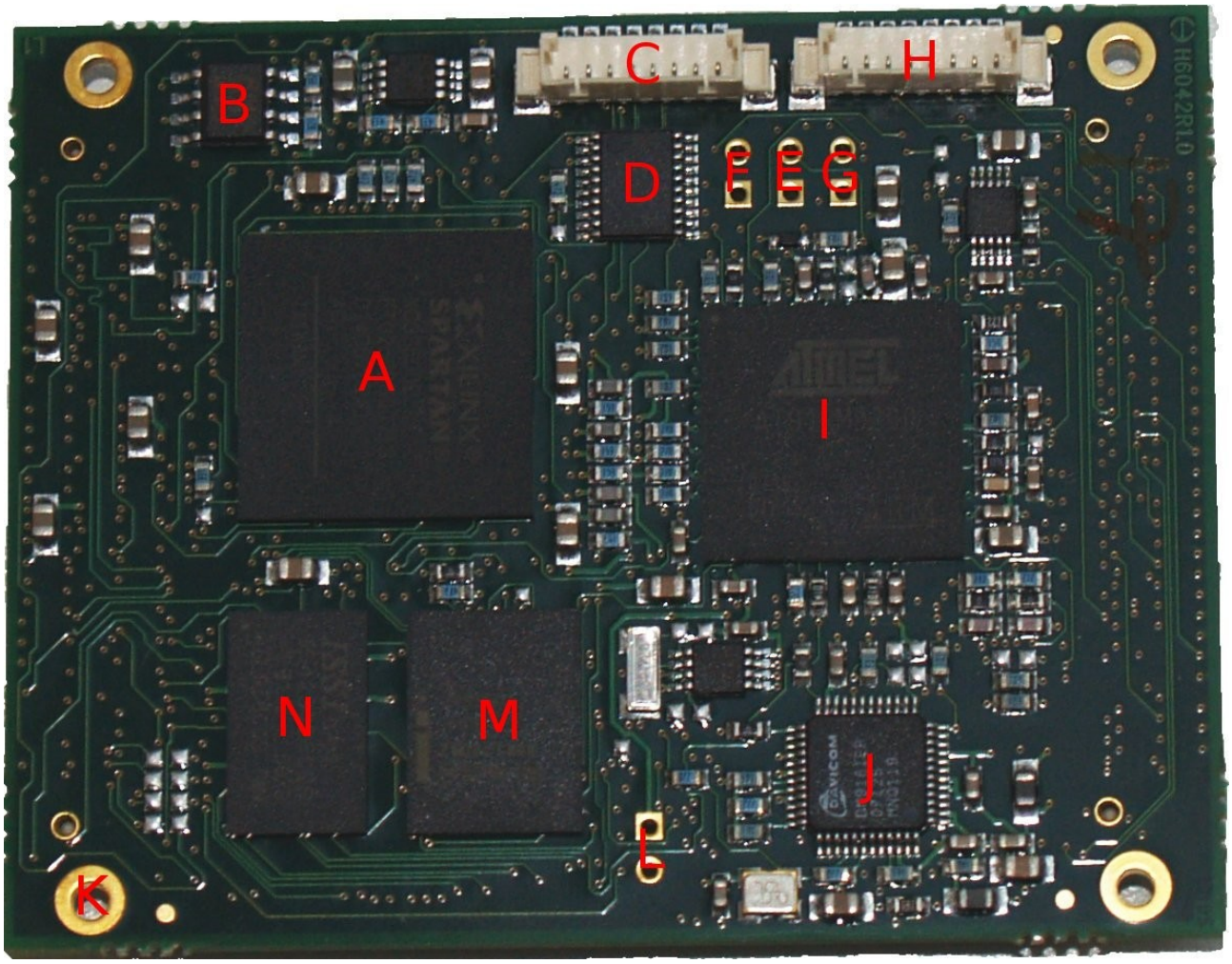

Figure 1: Computer module, top side view

Function/connector	Description
A	Spartan 3E FPGA
B	Core power regulation
C	FPGA JTAG
D	FPGA configuration flash
E	Boot Mode Select strap
F	+3.3V power
G	Serial debug RX/TX
H	ARM JTAG
I	AT91RM9200 ARM CPU
J	Davicom Ethernet PHY
K	Mounting holes (not connected to GND nor used for GND filtering)
L	Optional RTC battery connector
M	Intel P30 NOR flash

N	ISSI SDRAM

Table 3: Overview of H6042 functions and connectors, top side

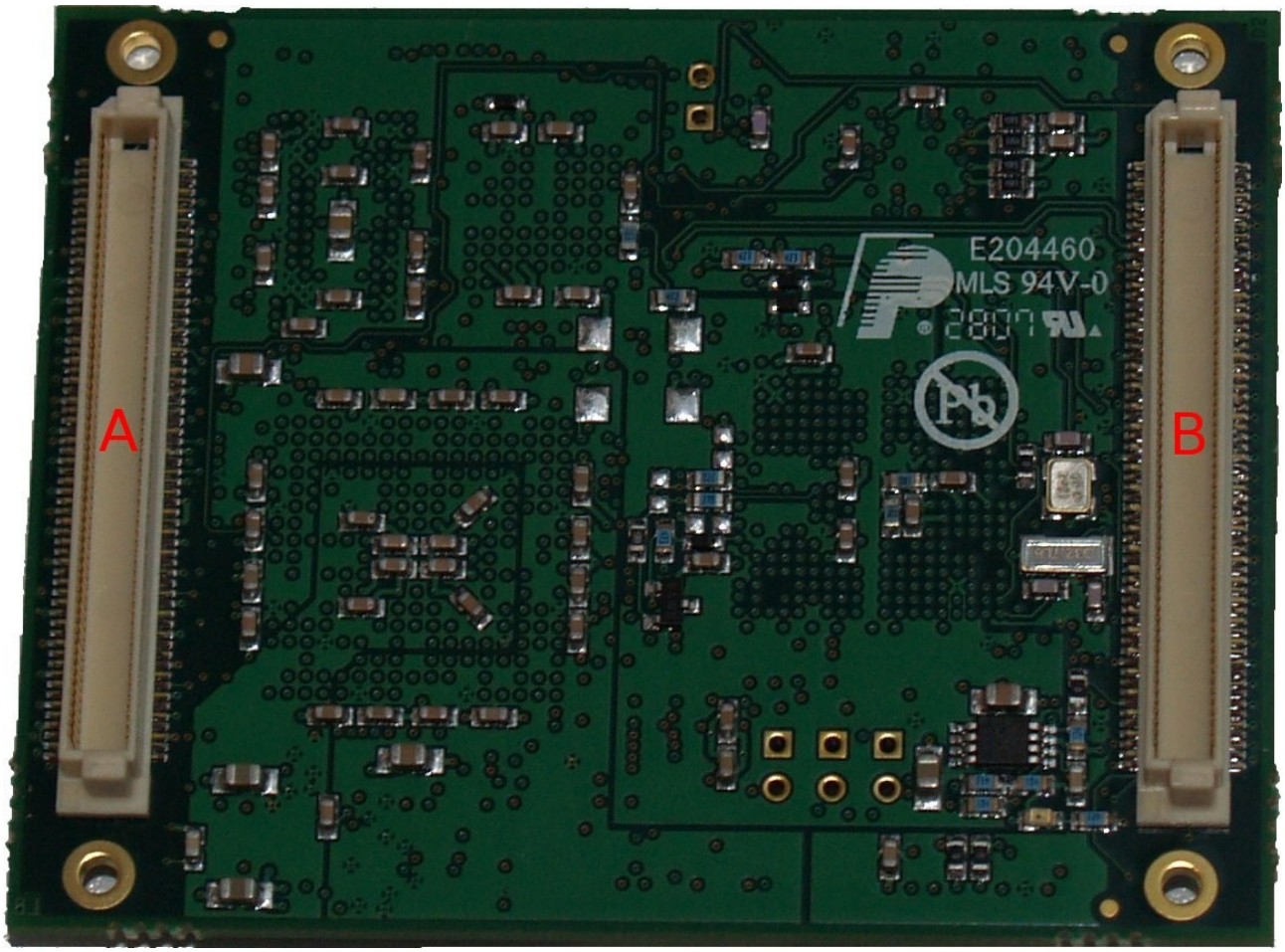

Figure 2: Computer module, bottom side view

Function/connector	Description
A	FPGA I/O. Signals have PCI interface impedance and length matching
B	ARM I/O.

Table 4: Overview of H6042 functions and connectors, bottom side

3.2 Models and options

Model	Description
H6042-04	H6042 without any FPGA mounted.
H6042-03	The FPGA on the board is a Xilinx Spartan3E-250
H6042-01	The FPGA on the board is a Xilinx Spartan3E-500

H6042-02	The FPGA on the board is a Xilinx Spartan3E1200

Table 5: H6042 CCOs/Models

3.3 Carrier boards

Model	Description
H4090	Reference carrier board, gives easy access to peripherals with standard connectors.

Table 6: Carrier boards.

4 Product specifications

4.1 Mechanical

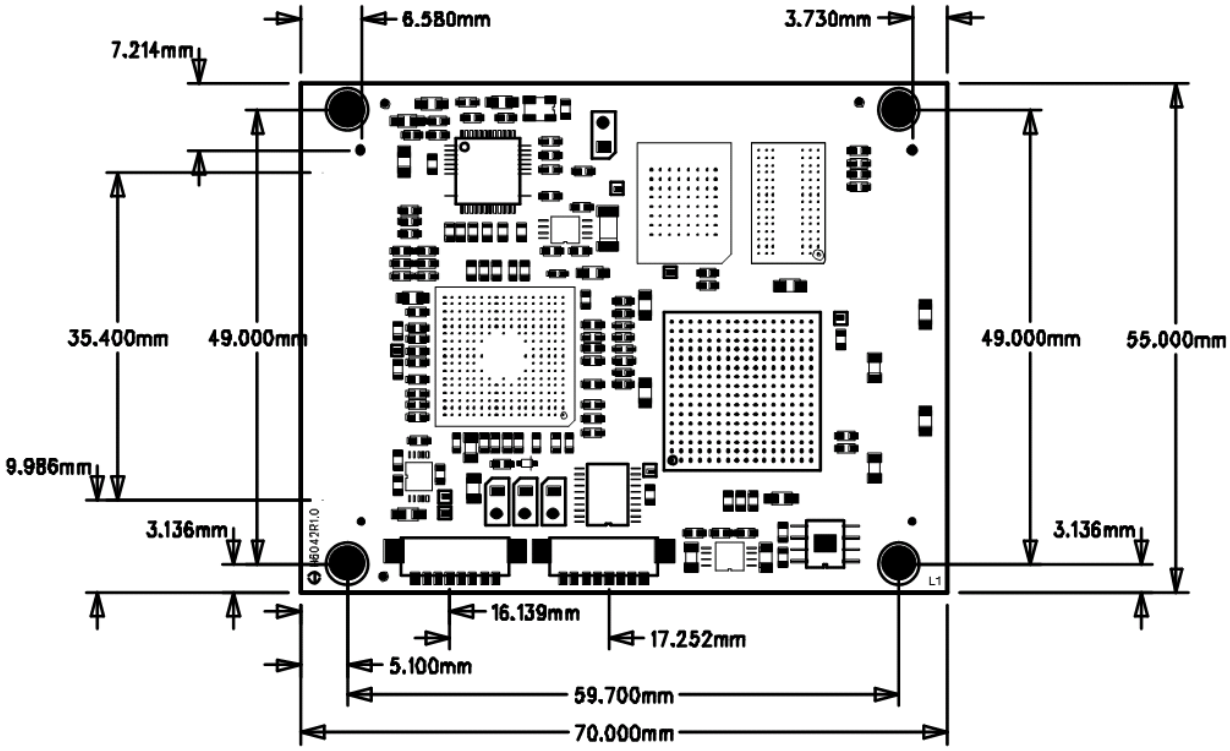

Figure 3: Mechanical drawing, top side view

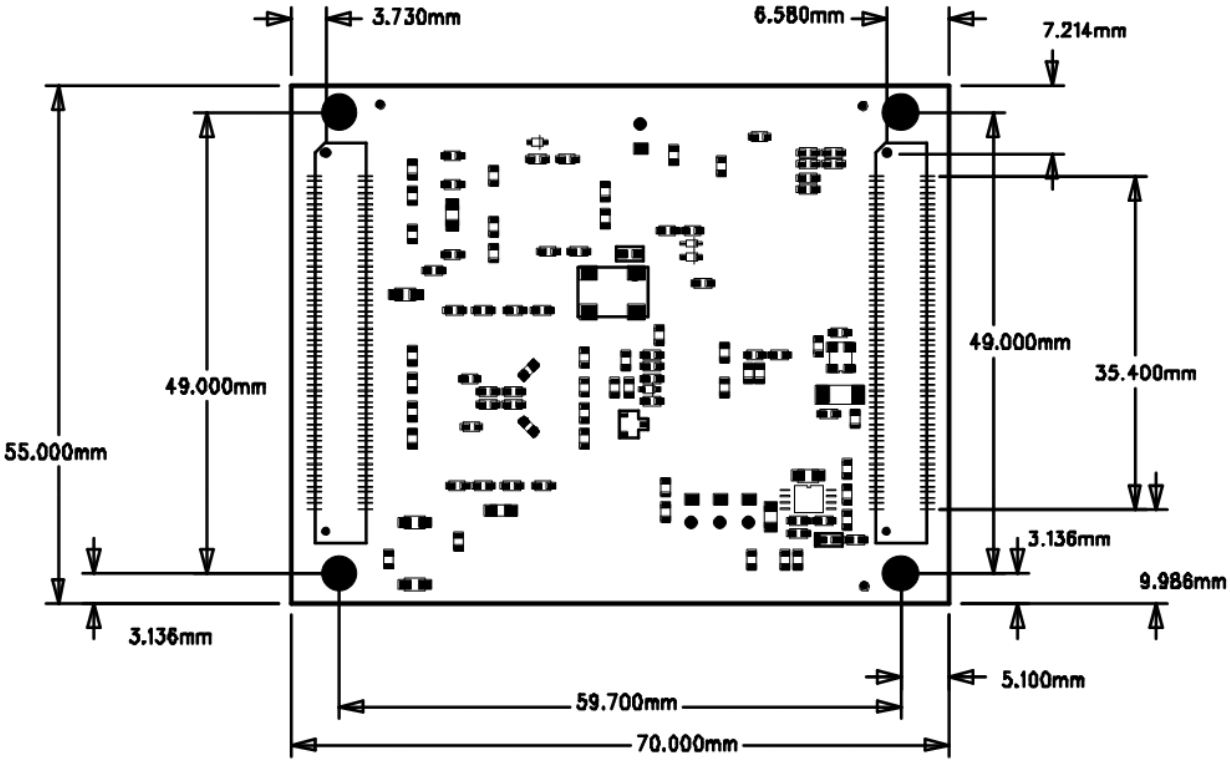

Figure 4: Mechanical drawing, bottom side view

4.1.1 Carrier board mounting

The board-to-board connectors give enough mechanical support in environments without extreme mechanical shocks. If the module is used in an extremely violent environment, the four mounting holes should be used. The mounting holes are not connected to ground on the H6042 module, nor used for filtering.

For high ESD protection, the screws should not be connected to chassis or outer structure, since the mounting holes' plating or pads do not have sufficient gaps to other signals and planes.

4.1.2 Component heights

Board-to-board stacking height is 5mm. Max component height on the CPU board is 2mm on bottom side, and 1.5mm on top side, excluding connectors and jumper pins J4, J7, J21 (aprx 10mm), J6, J3 (aprx 5mm) without a mating connector attached.

No hot components should be placed below or above the CPU board.

4.2 Electrical

4.2.1 Power supply requirements

The H6042 requires the power supply sources to be within voltage ranges to work properly.

Supply	Min	Max	Unit
VCC +3.3V	3.2	3.4	V
VCC +3.0V RTC backup battery	1.8	5.5	V

Table 7: Power supply.

4.2.2 Power consumption

The power consumption is dependent of the system configuration. Running software Processor load and speed mode, memory and attached devices. For the H6042 module the configuration (CCO) have heavy impact on the power consumption. The size of the FPGA is the reason for the major difference.

Module	Max dissipation at 3.3V	Typical dissipation at 3.3V	Unit
H6042 with Spartan3E250	455	285	mA
H6042 with Spartan3E500	500	300	mA
H6042 with Spartan3E1200	705	345	mA

Table 8: Power consumption.

The dissipation numbers are theoretical calculated values.

4.3 Thermal

In operating areas where the board is surrounded by air there is no need for nor active cooling or passive heat sink.

5 Board description

5.1 Block diagram

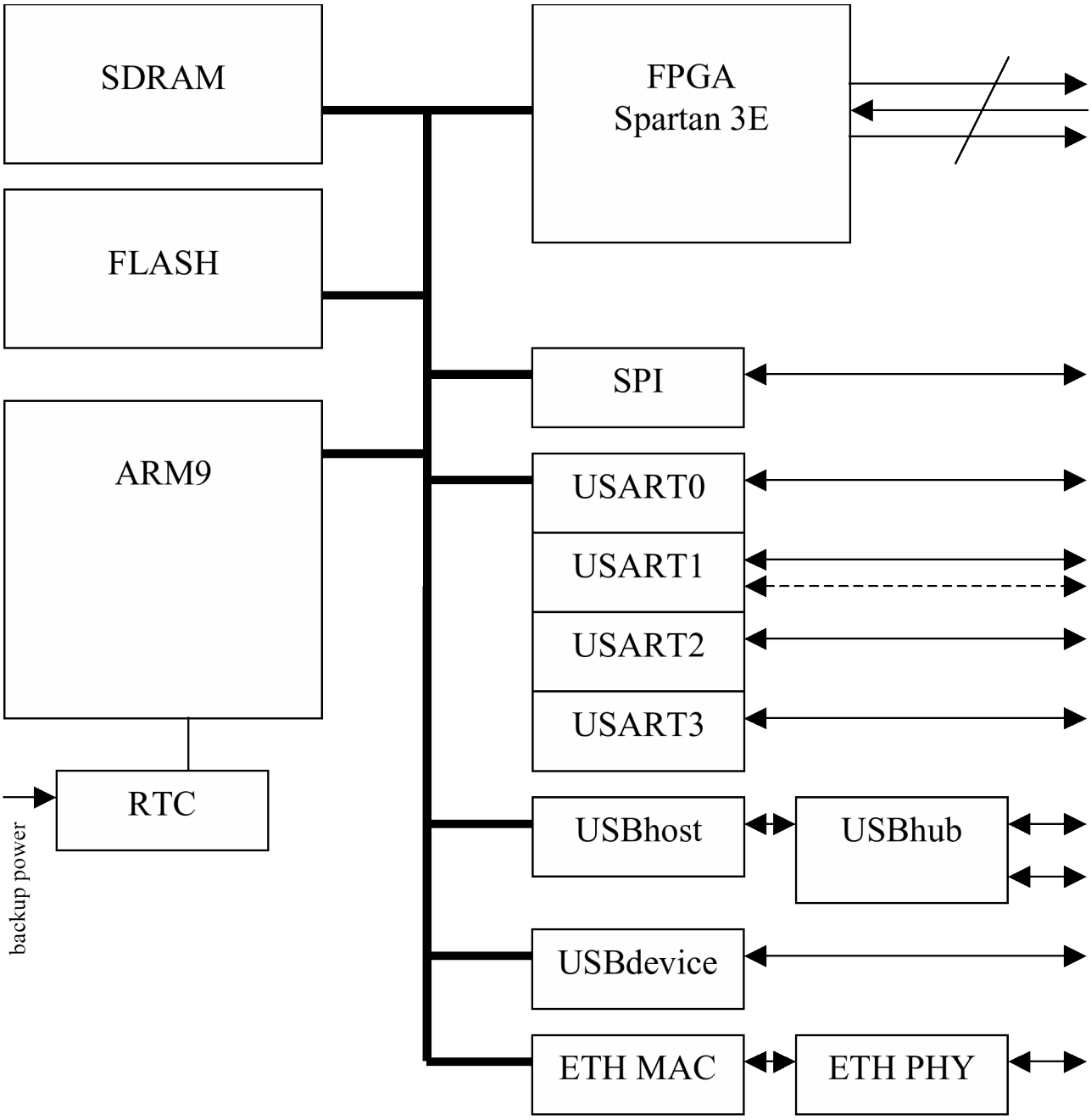

Figure 5: Module block diagram

5.2 ARM9 CPU

The CPU on the H6042 is an Atmel AT91RM9200. The processor is an ARM920T based CPU running at 180MHz, 200 MIPS.

5.3 SDRAM

256Mbit, (32Mbyte) mobile SDRAM.

5.4 FLASH

128Mbit, (16Mbyte) Intel strata P30 embedded flash. There is an option to mount 256 Mbit (32 Mbyte) flash.

5.5 FPGA, Spartan 3E

H6042 is a equipped with a Spartan 3E FPGA. The FPGA is not pre-configured.

Contact Hectronic for availability on different IP-blocks

The H6042 is designed for three FGPA-sizes: Spartan XC3S250E, XC3S500E and XC3S1200E. H6042 may also run without a FPGA mounted.

5.5.1 FPGA development

To develop contents for the FPGA a development tool from Xilinx is needed, called ISE.

There is a free version of the ISE, called ISE webPACK, which can be downloaded from [3].

5.5.2 Programming the FPGA PROM

The contents of the FPGA is stored in a PROM on the H6042.

Programming the FPGA PROM is done using a JTAG programmer. The JTAG signals (TDI, TDO, TCK, TMS) are located on the J3 on the H6042.

5.6 SPI - Serial Peripheral Interface

The interface supports communication with serial external devices. Four chip selects. External decoder may be implemented in FPGA.

SPI may be used to communicate with serial memories, such as DataFlash and 3-wire EEPROMs, and serial peripherals such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors External co-processors, and the onboard Spartan3E FPGA. Master and slave SPI mode is supported.

5.7 I2C

Two-wire Interface, aka I2C, compatibility with standard two-wire serial memory is supported.

5.8 USART0

The USARTs has Programmable Baud Rate Generator. 5- to 9-bit full-duplex synchronous or asynchronous serial communications. 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode. Parity generation and error detection. Framing error detection, overrun error detection.

USART0 implements TX, RX, RTS, CTS, and may be used for RS485 and RS232.

5.9 USART1

USART1 implements full RS232 modem signalling.

5.10 USART2

USART2 implements TX, RX, RTS, CTS, and may be used for RS485 and RS232.

Note that the RTS and CTS signals are also used for a Debug port RX, TX, which means that either function must be selected.

5.11 USART3

USART3 implements TX, RX, RTS, CTS, and may be used for RS485 and RS232.

5.12 USB host and USB hub

Compliance with Open HCI Rev 1.0 specification. Compliance with USB V2.0 Full-speed and Low-speed specification. Supports both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices. The USB root hub integrates two downstream USB ports.

5.13 USB device

USB V2.0 full-speed compliant, 12 Mbits per second. Embedded USB V2.0 full-speed transceiver. Embedded dual-port RAM for endpoints.

Suspend/Resume logic Ping-pong mode (two memory banks) for isochronous and bulk endpoints. Six general-purpose endpoints.

Endpoint 0, Endpoint 3: 8 bytes, no ping-pong mode

Endpoint 1, Endpoint 2: 64 bytes, ping-pong mode

Endpoint 4, Endpoint 5: 256 bytes, ping-pong mode

5.14 ETH MAC, Ethernet Medium Access Control, 10/100 controller

Compatibility with IEEE Standard 802.3

10 and 100Mbits per second data throughput capability. Full- and half-duplex operation. MII or RMII interface to the physical layer. Register interface to address, status and control registers. DMA interface, operating as a master on the Memory Controller. Interrupt generation to signal receive and transmit completion. 28-byte transmit and 28-byte receive FIFOs. Automatic pad and CRC generation on transmitted frames. Address checking logic may recognize four 48-bit addresses. Supports promiscuous mode where all valid frames are copied to memory. Supports physical layer management through MDIO interface.

5.15 ETH PHY, Ethernet Physical layer

A Low-power transceiver for 100BASE-TX and 10BASE-T PHY is mounted on the H6042. On the media side, it provides a direct interface either to Unshielded Twisted Pair Cable 5 (UTP5) for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. The PHY supports auto-negotiation function utilizing automatic media speed and protocol selection.

5.16 RTC, Real Time Clock with battery backup input

The real-time clock is a low-power clock/calendar. Address and data are transferred serially through an I^2C bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. If backup power is supplied to the VCC 3.3V Bat pin, the clock is ticking when the rest of the CPU board is not powered.

6 FPGA interface

6.1 FPGA access

The FPGA is accessed from the ARM CPU using the "static memory controller", the timing and access modes are described in chapter 18 of [2].

6.2 Memory bus mapping

The following table describes hos the FPGA is connected to the ARM CPU.

ARM signal	FPGA I/O pin	Description
CFOE/NRD	R11	Read signal
CFWE/NWE	N12	Write enable
CFIOR/NWR1	P11	Write signal
BFCS/NCS0	E14	Chip select 0 (Used by flash)
SDCS/NCS1	M13	Chip select 1 (Used by SDRAM)
NCS2	B6/M14	Chip select 2 (free)
ADDR[0]	G12	Address bus bit 0
ADDR[1]	J16	Address bus bit 1
ADDR[2]	K16	Address bus bit 2
ADDR[3]	J13	Address bus bit 3
ADDR[4]	J14	Address bus bit 4
ADDR[5]	H14	Address bus bit 5
ADDR[6]	H15	Address bus bit 6
ADDR[7]	H11	Address bus bit 7
ADDR[8]	H12	Address bus bit 8
ADDR[9]	G16	Address bus bit 9
ADDR[10]	G15	Address bus bit 10
ADDR[11]	G14	Address bus bit 11
ADDR[12]	G13	Address bus bit 12
ADDR[13]	F15	Address bus bit 13
ADDR[14]	F14	Address bus bit 14
ADDR[15]	E16	Address bus bit 15
ADDR[16]	E13	Address bus bit 16
ADDR[17]	N14	Address bus bit 17

ADDR[18]	L13	Address bus bit 18
ADDR[19]	L12	Address bus bit 19
ADDR[20]	H3	Address bus bit 20
ADDR[21]	J3	Address bus bit 21
ADDR[22]	J4	Address bus bit 22
ADDR[23]	T8	Address bus bit 23
ADDR[24]	R4	Address bus bit 24
ADDR[25]	P13	Address bus bit 25
DATA[0]	R15	Data bus bit 0
DATA[1]	R16	Data bus bit 1
DATA[2]	P15	Data bus bit 2
DATA[3]	P16	Data bus bit 3
DATA[4]	F12	Data bus bit 4
DATA[5]	F13	Data bus bit 5
DATA[6]	M16	Data bus bit 6
DATA[7]	N16	Data bus bit 7
DATA[8]	D14	Data bus bit 8
DATA[9]	D15	Data bus bit 9
DATA[10]	L15	Data bus bit 10
DATA[11]	L14	Data bus bit 11
DATA[12]	K12	Data bus bit 12
DATA[13]	K13	Data bus bit 13
DATA[14]	K14	Data bus bit 14
DATA[15]	K15	Data bus bit 15

Table 9: Mapping between FPGA and ARM memory bus.

6.3 Example VHDL code

In the fpga directory in the BSP of the H6042 there is a sample ISE project and VHDL code. This code is a simple extension of some I/O pins of the FPGA to the ARM CPU. There is also a driver for Linux which allows an usermode application to access the I/O pins. The compilation of the FPGA core and programming of the FPGA must be done manually.

7 Quality and environmental data

7.1 Required environmental conditions

Temperature ambient, operating	-40 to +80 ºC
Temperature ambient, storage	-40 to +80 ºC

Table 10: Environmental contidions.

7.2 EMC compliance

When correctly installed in a suitable chassis with recommended filtering on carrier-board as described in the design guidelines, the H6042 is designed to meet the following EMC regulations.

EN50081-1 Generic emission standard for residential commercial and light industry use.

CISPR25 RF-disturbances for vehicles (e-type approval).

7.3 Safety compliance

Depending on carrier board design, and mechanic casing.

7.4 Industry standard compliances

The H6042 implements the following industry standards. To fulfil the standards some filtering/drivers are needed on the carrier board.

Standard	Description	Reference
USB 2.0	Universal Serial Bus rev 2.0	http://www.usb.org
IEEE 802.3i[1]	Ethernet 10Base-T	http://www.ieee.org
IEEE 802.3u[1]	Fast Ethernet 100Base-Tx	http://www.ieee.org
I2C	Inter-Integrated Circuit bus	NXP (formerly Philips) I^2C 2.1 specification (January 2000)
SPI	Serial Peripherial Interface BUS	No formal spec. exists. First introduced by Freescale (formerly Motorola)
RS232/485/422[2]	Serial communication standards	ANSI/TIA/EIA and the international equivalent from ITU
IEEE 1149.1	JTAG Boundary Scan (ARM CPU)	http://www.ieee.org

Table 11: Industry standards implemented by the H6042.

[1] Requires Ethernet trafo on carrier board.

[2] The linedriver circuitery is to be placed on the carrier board. H6042 hosts the UARTs.

7.5 Quality ensures and milieu influences

RoHS compliant

ISO9001

ISO14001

7.5.1 WEEE 2002/96/EC

The H6042 is intended to be included in a product. The responsibility when it comes to recycling and registering the end product with the correct authorities lies at the producer of the end product.

8 Design guide lines

This section contains some hints when designing a carrier board for the H6042.

8.1 Buses

8.1.1 USB

The USB device detect signal (J2.105) should be connected to the + 5V on the USB device connector. The H6042 doesn't use it for power supply, only to detect that the host is present.

In [2], chapter 34 and 35 the USB interface is described.

8.1.2 Ethernet

The ethernet RX/TX signals from the H6042 must be completed with magnetics before connected to a RJ45 connector. It is also possible to use an RJ45 socket with integrated magnetics.

The ethernet status signals ETH link/act, ETH duplex, ETH speed may be connected to a LED. The LED should be connected from +3.3 V through a 330 ohm resistor to the status signal.

In [2], chapter 36 the ethernet interface is described.

8.1.3 I2C

The I^2C bus is available at J2 pins marked with TWCK and TWD. TWCK is the I^2C clock, and TWD is the I^2C data.

In [2], chapter 29 the I^2 interface is described.

8.1.4 SPI

The AT91RM9200 has a bug in the CS0 for SPI, so this chip select should not be used. Use CS1-CS3 instead.

In [2], chapter 28 the SPI interface is described.

8.1.5 PCI

This is only applies if the PCI interface is implemented in the FPGA.

The PCI bus is sensitive of timing and impedance, see the PCI local bus specification for recommendations of routing PCI signals.

8.1.6 LCD

This is only applies if the LCD interface is implemented in the FPGA.

The LCD interface is sensitive of timing and impedance, see the specification for recommendations of

routing LCD signals.

8.1.7 CAN

This is only applies if the CAN interface is implemented in the FPGA.

The CAN RX/TX signals must be completed with a line driver before connected to a CAN bus.

8.2 Devices

8.2.1 Debug UART

The RX/TX lines of the debug console is shared with RTS/CTS of USART2, which meas that either function must be selected

The debug UART is mandatory to be able to communicate with the firmware. When the firmware is installed and configured it is possible to do without the debug UART. But for development purposes it is recommended that the debug UART is used.

8.2.2 ARM PA31

The GPIO PA31 is the BMS (boot mode select) which is sampled by the AT91RM9200 at boot time, if the PA31 is asserted high the AT91RM9200 will go into a "download firmware" state. To ensure normal operation, leave this pin in high impedance state during boot up.

8.2.3 GPIO

Many of the I/O pins on the AT91RM9200 CPU has multiple functions, the connector table for J2 (pins marked with class "alog") shows all functions that are available on the H6042.

8.2.4 FPGA

The FPGA pins that are available shown in the tables for J1 and J2 (pins makrked with class "slog"). Some of the FPGA pins have multiple functionality (such as PCI, LCD or CAN), but if these features aren't implemented in the FPGA the pins may be used for anything.

8.2.5 RTC

There is a RTC on the H6042, connected to the AT91RM9200 via the I2C bus. Optionally the RTC can connected to a backup battery through the sb3v / BAT pin on connector J1.

8.2.6 Power good signals

Don't attempt to drive these pins (either high or low), since this may inhibit the H6042 to boot.

8.3 Power supply

8.3.1 +3.3 V

The +3.3 V power supply on the carrier board must be able to provide as much current as specified in the power consumption table.

8.3.2 +5 V

The +5 V connections on J1 are not used internally on the H6042. However the +5 V pins on J1 are tied together on the H6042.

Appendix A Firmware reference

A.1 Bootloader, U-boot

U-boot is a bootloader supporting boot from flash, USBmemory, Ethernet and serialport. The purpose of the bootloader is to bring the target board to a state where an operating system can be loaded and executed. This means that U-boot does some basic hardware initializations (PLL:s, SDRAM, UART:s, network devices, etc).

H6042 is shipped with U-boot installed in the flash memory.

A.2 Bootstrap

The Bootstrap is the procedure to program the bootloader to the H6042.

Two versions of U-boot are actually needed. One version doing the initialisations described in [2], and another version not doing these initialisations. Let's call the latter u-boot-h6042-latest-no_hwinit.bin and t (more complete) u-boot-h6042-latest.bin.

The Bootstrap mode is entered when the BMS-pin is active, at bootstrap the communication is done by the debug serial port.

The steps involved to do the bootstrapping are:

1. Upload loader.bin to the target board's SRAM using sx-at91. This initiates the target board's SDRAM memory and initiates another xmodem receive sequence that places the next transfer in SDRAM.
2. Upload u-boot-h6042-latest-no_hwinit.bin into SDRAM. Note that this is not the u-boot version that we we want to put into flash memory. Since loader.bin did the necessary initialisation of the hardware, u-boot must not do that.
3. Start a terminal emulator on the connected serial port.
4. Use the command line interface to download u-boot-h6042-latest.bin to SDRAM.
5. Write u-boot-h6042-latest.bin to flash memory.

A.3 U-boot Setup configuration, default setup, update

Please reefer to U-boot documentation, and Hectronic SW application notes and getting started guides to get details about these subjects.

There are more information about U-boot in the Helix documentation.

Appendix B Connectors and pinouts

B.1 Connector placements

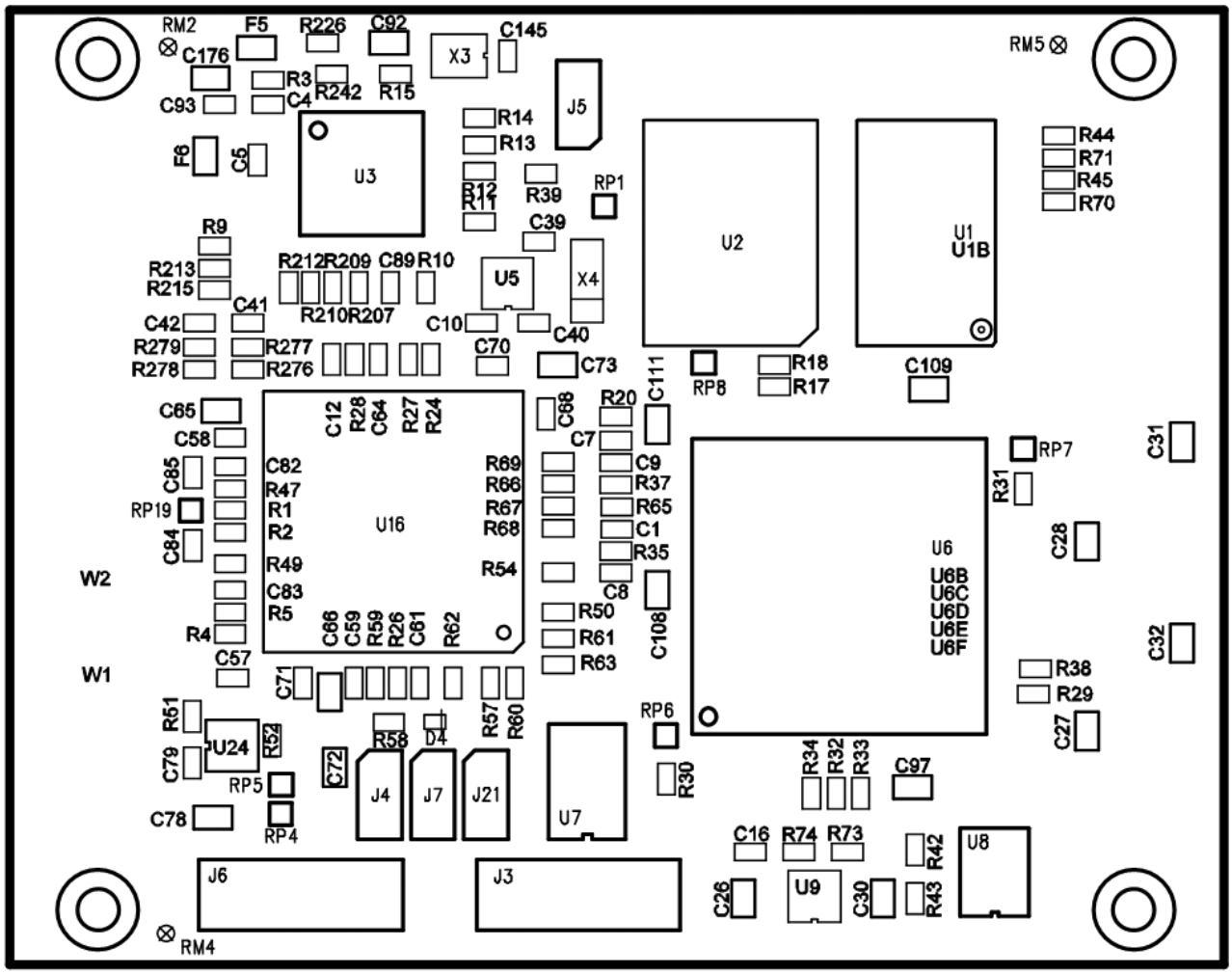

Figure 6: Connector and component placement, top side view

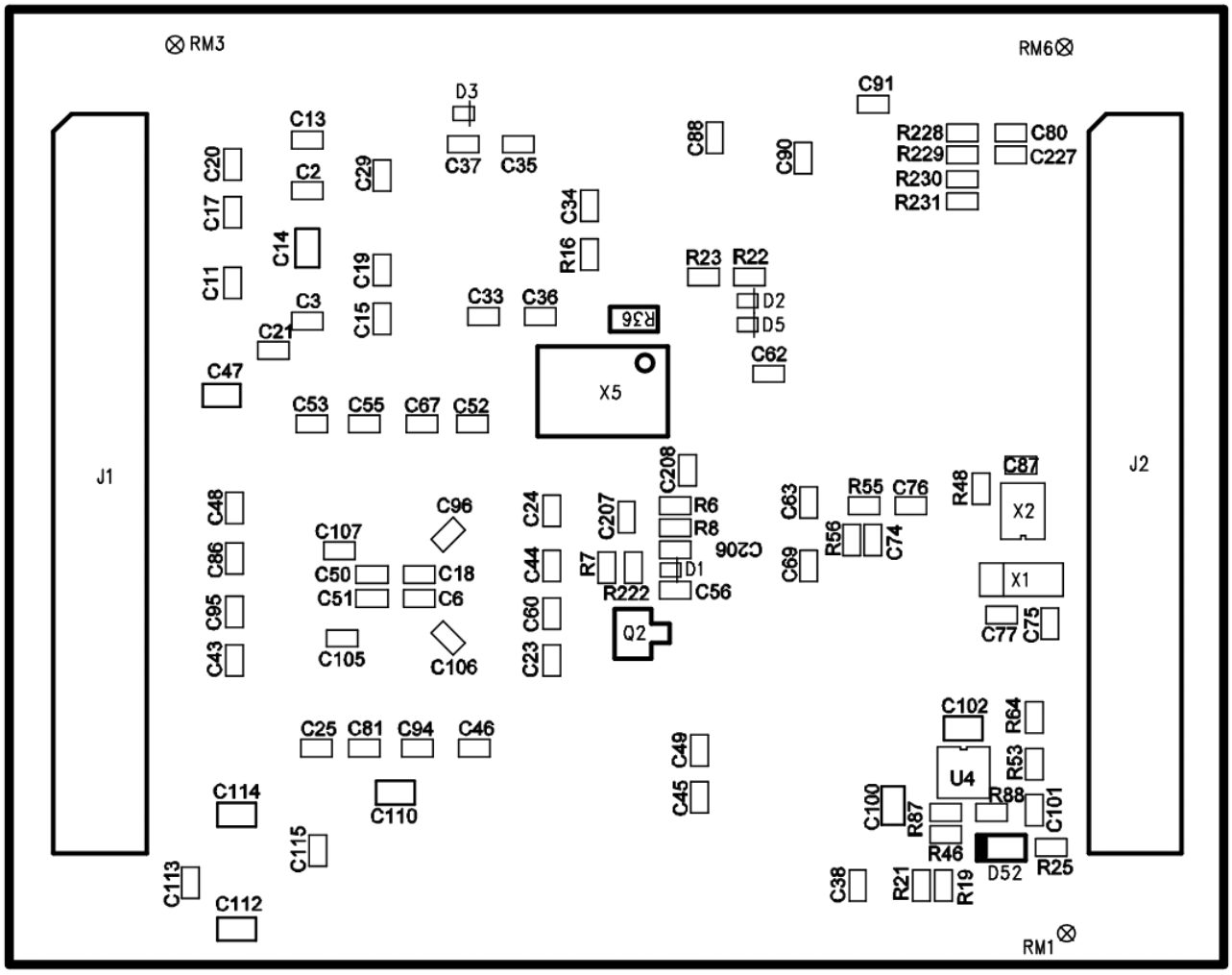

Figure 7: Connector and component placement, bottom side view

B.2 J3 - JTAG Spartan 3E FPGA

Molex 53398-0890

Placement 1290 x 63 from origo corner (mils)

pin#	signal	class
1	TDI	slog
2	TMS	slog
3	TCK	slog
4	TDO	slog
5		
6		
7	VCC 2v5	pow
8	GND	pow

Table 12: J3 pinout.

B.3 J2 - ARM/FPGA

Hirose FX8C-120P-SV(71) (used on CPU board)

Hirose FX8C-120S-SV(71) (used on carrier board)

Placement 200 x 1090 from origo corner (mils)

pin#	signal	class	pin#	signal	class
1	ETH TX+	eth	2	ETH RX+	eth
3	ETH TX-	eth	4	ETH RX-	eth
5	ARM PC6 (wait-)	alog	6	VCC +3.3v eth	ethp
7	ETH link/act	ethl	8	ETH duplex	ethl
9	ETH linkstatus	ethl	10	ETH speed-	ethl
11	TWCK (I2C CLK)	alog	12	ARM PA31 (BMS)	bms
13	TWD (I2C DAT)	alog	14	EXT RESET	rst
15	USB0 D+	usb	16	USB1 D+	usb
17	USB0 D-	usb	18	USB1 D-	usb
19	gnd	pow	20	gnd	pow
21			22	FPGA M8	slog
23	ARM PA19/USART0 CLK	alog	24	FPGA L8	slog
25	ARM PA17/USART0 TX	alog	26	ARM PA18/USART0 RX	alog
27	ARM PA21/USART0 RTS	alog	28	ARM PA20/USART0 CTS	alog
29	ARM PB22/USART1 CLK	alog	30	ARM PB21/USART1 RX	alog
31	ARM PB20/USART1 TX	alog	32	ARM PB24/USART1 CTS	alog
33	ARM PB26/USART1 RTS	alog	34	ARM PB23/USART1 DCD	alog
35	ARM PB19/USART1 DTR	alog	36	ARM PB25/USART1 DSR	alog
37	ARM PA24/USART2 CLK	alog	38	ARM PB18/USART1 RI	alog
39	gnd	pow	40	gnd	pow
41	ARM PA23/USART2 TX	alog	42	ARM PA22/USART2 RX	alog
43	ARM PA31/USART2 RTS/dbg TX	alog	44	ARM PA30/USART2 CTS/dbg RX	alog
45	ARM PB2/USART3 CLK/SSC TDO	alog	46	ARM PA6/USART3 RX/SPI NPCS3	alog
47	ARM PA5/USART3 TX/SPI NPCS2	alog	48	ARM PB1/USART3 CTS/SSC TK0	alog
49	ARM PB0/USART3 RTS/SSC TF0	alog	50	ARM PA2/SPI SPCK	alog
51	ARM PA0/SPI MISO	alog	52	ARM PA1/SPI MOSI	alog
53	ARM PA3/SPI NPCS0	alog	54	ARM PA4/SPI NPCS1	alog
55	ARM PA27/MMC MCCK	alog	56	ARM PB3/MMC MCDA1/SSC RD0	alog
57	ARM PA28/MMC MCCDA	alog	58	ARM PB4/MMC MCDA2/SSC RK0	alog
59	gnd	pow	60	gnd	pow
61	ARM PA29/MMC MCDA0	alog	62	ARM PB5/MMC MCDA3/SSC RF0	alog
63	ARM PB6/SSC TF1	alog	64	ARM PB12/SSC TF2	alog
65	ARM PB7/SSC TK1	alog	66	ARM PB13/SSC TK2	alog
67	ARM PB8/SSC TD1	alog	68	ARM PB14/SSC TD2	alog
69	ARM PB9/SSC RD1	alog	70	ARM PB15/SSC RD2	alog

71	ARM PB10/SSC RK1	alog	72	ARM PB16/SSC RK2	alog
73	ARM PB11/SSC RF1	alog	74	ARM PB17/SSC RF2	alog
75	ARM PB29/IRQ0	int	76	ARM PB28/FIQ	int
77	ARM PD7/PCK0	alog	78	ARM PD9/PCK2	alog
79	gnd	pow	80	gnd	pow
81	ARM PD8/PCK1	alog	82	ARM PD10/PCK3	alog
83	CAN RX/FPGA C16	slog	84	LCD DOTCLK/FPGA P9	slog
85	CAN TX/FPGA C15	slog	86	LCD D0/FPGA C8	slog
87	LCD D16/FPGA A7	slog	88	LCD D1/FPGA D8	slog
89	LCD D17/FPGA P14	slog	90	LCD D2/FPGA E9	slog
91	LCD SYNC/FPGA N8	slog	92	LCD D3/FPGA A9	slog
93	LCD HSYNC/FPGA N9	slog	94	LCD D4/FPGA D10	slog
95	LCD DEN/FPGA R13	slog	96	LCD D5/FPGA E10	slog
97	LCD CC (contrast)/FPGA T13	slog	98	LCD D6/FPGA C11	slog
99	gnd	pow	100	gnd	pow
101	USB device D+	usb	102	LCD D7/FPGA B11	slog
103	USB device D-	usb	104	LCD D8/FPGA D11	slog
105	USB device detect	pusb	106	LCD D9/FPGA E11	slog
107	pwrgd	alog	108	LCD D10/FPGA B13	slog
109	pwrgd ps	alog	110	LCD D11/FPGA A13	slog
111	ARM JTAG TCK	alog	112	LCD D12/FPGA B14	slog
113	ARM JTAG TMS	alog	114	LCD D13/FPGA A14	slog
115	ARM JTAG TDI	alog	116	LCD D14/FPGA D9	slog
117	ARM JTAG TDO	alog	118	LCD D15/FPGA A12	slog
119	gnd	pow	120	gnd	pow

Table 13: J2 pinout.

B.4 J1 - PCI/IO header

Hirose FX8C-120P-SV(71) (used on CPU board)

Hirose FX8C-120S-SV(71) (used on carrier board)

Placement 2550 x 1090 from origo corner (mils)

pin#	signal	class	pin#	signal	class
1	PCI idsel1 (not connected on H6042r10)		2	FPGA JTAG TDI	slog
3	FPGA JTAG TCK	slog	4	FPGA JTAG TDO	slog
5	gnd	pow	6	FPGA JTAG TMS	slog
7	PCI clkrun-(not connected on H6042)		8	PCI idsel0/FPGA G5	slog
9	+5v (not connected on H6042)		10	+5v (not connected on H6042)	
11	+5v (not connected on H6042)		12	PCI inta-/FPGA E7	slog

13	PCI intb- (not connected on H6042)		14	PCI intc- (not connected on H6042)	
15	PCI intd- (not connected on H6042)		16	+5v (not connected on H6042)	
17	PCI req3- (not connected on H6042)		18	PCI clk2 (not connected on H6042)	
19	PCI req1- (not connected on H6042)		20	+5v (not connected on H6042)	
21	PCI gnt3- (not connected on H6042)		22	PCI clk3 (not connected on H6042)	
23	gnd	pow	24	gnd	pow
25	gnd	pow	26	gnd	pow
27	PCI clk1 (not connected on H6042)		28	PCI gnt1- (not connected on H6042)	
29	gnd	pow	30	PCI rst-/FPGA E1	slog
31	PCI clk0/FPGA F9	slog	32	+5v (not connected on H6042)	
33	gnd	pow	34	PCI gnt0-/FPGA H5	slog
35	PCI req0-/FPGA C6	slog	36	gnd	pow
37	+5v (not connected on H6042)		38	PCI req2- (not connected on H6042)	
39	PCI ad31/FPGA A4	slog	40	PCI ad30/FPGA A5	slog
41	PCI ad29/FPGA B4	slog	42	+3.3v	pow
43	gnd	pow	44	PCI ad28/FPGA C4	slog
45	PCI ad27/FPGA C5	slog	46	PCI ad26/FPGA C3	slog
47	PCI ad25/FPGA B2	slog	48	gnd	pow
49	+3.3v	pow	50	PCI ad24/FPGA B1	slog
51	PCI cbe3-/FPGA G4	slog	52	PCI gnt2- (not connected on H6042)	
53	PCI ad23/FPGA C2	slog	54	+3.3v	pow
55	gnd	pow	56	PCI ad22/FPGA C1	slog
57	PCI ad21/FPGA F5	slog	58	PCI ad20/FPGA E4	slog
59	PCI ad19/FPGA E3	slog	60	gnd	pow
61	+3.3v	pow	62	PCI ad18/FPGA F4	slog
63	PCI ad17/FPGA F3	slog	64	PCI ad16/FPGA D1	slog
65	PCI cbe2-/FPGA G2	slog	66	+3.3v	pow
67	gnd	pow	68	PCI frame-/FPGA H6	slog
69	PCI irdy-/FPGA H4	slog	70	gnd	pow
71	+3.3v	pow	72	PCI trdy-/FPGA J2	slog
73	PCI devsel-/FPGA J5	slog	74	gnd	pow
75	gnd	pow	76	PCI stop-/FPGA K1	slog
77	PCI lock- (not connected on H6042)		78	+3.3v	pow
79	PCI perr-/FPGA J1	slog	80	PCI pcixap (not connected on H6042)	
81	+3.3v	pow	82	PCI m66en (not connected on H6042)	
83	PCI serr-/FPGA D6	slog	84	gnd	pow
85	+3.3v	pow	86	PCI par/FPGA G3	slog

87	PCI cbe1-/FPGA K3	slog	88	PCI ad15-/FPGA L2	slog
89	PCI ad14-/FPGA L3	slog	90	+3.3v	pow
91	gnd	pow	92	PCI ad13-/FPGA L5	slog
93	PCI ad12-/FPGA K5	slog	94	PCI ad11-/FPGA N1	slog
95	PCI ad10-/FPGA M1	slog	96	gnd	pow
97	gnd	pow	98	PCI ad09-/FPGA L4	slog
99	PCI ad08-/FPGA M4	slog	100	PCI cbe0-/FPGA K2	slog
101	PCI ad07-/FPGA N2	slog	102	+3.3v	pow
103	+3.3v	pow	104	PCI ad06-/FPGA P1	slog
105	PCI ad05-/FPGA P2	slog	106	PCI ad04-/FPGA R1	slog
107	PCI ad03-/FPGA R2	slog	108	gnd	pow
109	gnd	pow	110	PCI ad02-/FPGA P3	slog
111	PCI ad01-/FPGA N5	slog	112	PCI ad00-/FPGA P5	slog
113	+5v (not connected on H6042)		114	+5v (not connected on H6042)	
115	sb3v (not connected on H6042)		116	sb3v / BAT	
117	+5v (not connected on H6042)		118	+5v (not connected on H6042)	
119	+5v (not connected on H6042)		120	+5v (not connected on H6042)	

Table 14: J1 pinout.

B.5 J4 - Debug serial port

2.54 mm, jumper header

pin#	signal	class
1	TX debug	alog
2	RX debug	alog

Table 15: J4 pinout.

B.6 J7 - Boot Mode Select (BMS)

2.54 mm, jumper header

pin#	signal	class
1	3.3V	pow
2	BMS	bms

Table 16: J7 pinout.

B.7 J21 - Alternative power supply

2.54 mm, jumper header

pin#	signal	class
1	3.3V	pow

2	GND	pow

Table 17: J21 pinout.

B.8 J5 - Alternative Battery connection

2.54 mm, jumper header

pin#	signal	class
1	Bat+	bat
2	GND	pow

Table 18: J5 pinout.

B.9 J6 - JTAG ARM CPU

Molex 53398-0890

Placement 660 x 63 from origo corner (mils)

pin#	signal	class
1	VCC3v3	pow
2	TDO	alog
3	TDI	alog
4	PWR GOOD	powg
5	PWR GOOD PS	powg
6	TMS	alog
7	GND	pow
8	TCK	alog

Table 19: J6 pinout.

Appendix C Signal characteristics

Each signal in the pin signal listings have a class tag. Here follows descriptions of the different signal classes on the board.

C.1 bms - Boot Mode Select

The boot mode select is a configuration signal sampled at *external* reset. The pin is shared with a debug serial port on the CPU. To boot from the CPU-internal ROM and execute the X-modem download sequence, this signal is to be pulled up to 3.3V. In practice, connect a 8k2 resistor over pin1 and pin2 at the J7 connector.

C.2 pow - power line

This is a power supply (input) connection.

C.3 eth - Ethernet data signal

The Ethernet signals are differential pair signal. Length matching and differential impedance are critical parameters. A line transformer is needed before connecting to standard Ethernet cabling. A connector with integrated transformer may be used.

C.4 ethl - Ethernet LED status signal

These are the signals for status LEDs. Current limiting series resistors must be used.

C.5 ethp - Ethernet power

The Ethernet signals are differential pair signal. Length matching and

C.6 alog - ARM CPU logic level signal

ARM CPU logic level signal. Pins has a programmable pull-up resistor of 15kOhm. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that must be enabled as peripherals at reset. Signals is 3.3V logic level.

The full electric specification of the GPIO pins may be found in [2].

Maximum voltage that may be applied to these pins are 3.6V.

C.7 slog - Spartan 3E FPGA logic level signal

Spartan FPGA logic level signal. Depending on the FPGA firmware, the pins can either be input or output. Signals are 3.3V logic level.

Maximum voltage that may be applied to these pins are 4.3V.

C.8 rst - Reset input signal

External reset signal, pulse to ground to achieve a system reset. Signal should be high-impedance or open to let system run.

C.9 powg - Power good

Output signal from the H6043 power converter. This signal is asserted high when the 3.3 V and 1.8V are stable.

C.10 usb - USB data signal

The USB signals are differential pairs. Length matching, maximum length and differential impedance are critical design parameters. The pairs should be common mode filtered before cable connector to avoid conductive EMC problems.

C.11 pusb - USB device power input

The USB device power input signal is only used for detection of a connected host controller. A host controller should supply this pin with its 5V pin.

C.12 bat - RTC battery

RTC battery positive pole. This supplies the real time clock onboard H6042. Standby input current is <2uA.

Appendix D Interrupt, device and address assignments

D.1 Memory map

address [hex]	device	size [bytes]
0x0000 0000 - 0x000F FFFF	Boot memory	1M
0x0010 0000 - 0x001F FFFF	ROM	1M
0x0020 0000 - 0x002F FFFF	SRAM	1M
0x0030 0000 - 0x003F FFFF	USB Host	1M
	Undefined	
0x1000 0000 - 0x1FFF FFFF	EBI Chip select 0 / BFC	256M
0x2000 0000 - 0x2FFF FFFF	EBI Chip select 1 / SDRAMC	256M
0x3000 0000 - 0x3FFF FFFF	EBI Chip select 2	256M
0x4000 0000 - 0x4FFF FFFF	EBI Chip select 3 / NAND Flash Logic	256M
0x5000 0000 - 0x5FFF FFFF	EBI Chip select 4 / CF Logic	256M
0x6000 0000 - 0x6FFF FFFF	EBI Chip select 5 / CF Logic	256M
0x7000 0000 - 0x7FFF FFFF	EBI Chip select 6 / CF Logic	256M
0x8000 0000 - 0x8FFF FFFF	EBI Chip select 7 / CF Logic	256M
	Undefined	
0xF000 0000 - 0xFFF9 FFFF	Reserved	
0xFFFA 0000 - 0xFFFA 3FFF	TCO, TC1, TC2	16K
0xFFFA 4000 - 0xFFFA 7FFF	TC3, Tc4, TC5	16K
0xFFFA 8000 - 0xFFFA FFFF	Reserved	16K
0xFFFB 0000 - 0xFFFB 3FFF	UDP	16K
0xFFFB 4000 - 0xFFFB 7FFF	MCI	16K
0xFFFB 8000 - 0xFFFB BFFF	TWI	16K
0xFFFB C000 - 0xFFFB FFFF	EMAC	16K
0xFFFC 0000 - 0xFFFC 3FFF	USART0	16K

0xFFFC 4000 - 0xFFFC 7FFF	USART1	16K
0xFFFC 8000 - 0xFFFC BFFF	USART2	16K
0xFFFC C000 - 0xFFFC FFFF	USART3	16K
0xFFFD 0000 - 0xFFFD 3FFF	SSC0	16K
0xFFFD 4000 - 0xFFFD 7FFF	SSC1	16K
0xFFFD 8000 - 0xFFFD BFFF	SSC2	16K
0xFFFD C000 - 0xFFFD FFFF	Reserved	
0xFFFE 0000 - 0xFFFE 3FFF	SPI	16K
0xFFFE 4000 - 0xFFFF F0FF	Reserved	
0xFFFF F100 - 0xFFFF F1FF	AIC	512
0xFFFF F200 - 0xFFFF F3FF	DBGU	512
0xFFFF F400 - 0xFFFF F5FF	PIOA	512
0xFFFF F600 - 0xFFFF F7FF	PIOB	512
0xFFFF F800 - 0xFFFF F9FF	PIOC	512
0xFFFF FA00 - 0xFFFF FBFF	PIOD	512
0xFFFF FC00 - 0xFFFF FCFF	PMC	256
0xFFFF FD00 - 0xFFFF FDFF	ST	256
0xFFFF FE00 - 0xFFFF FEFF	RTC	256
0xFFFF FF00 - 0xFFFF FFFF	MC	256

Table 20: Memory map.

Appendix E Interrupt allocation

Appendix F Notational conventions and acronyms used

F.1 Notational conventions

All number are decimal unless otherwise stated.

Bit 0 is the low-order bit.

If a bit is set to 1, the associated description is true unless otherwise stated.

F.2 Acronyms

ESD - Electro Static Discharge

EMC - ElectroMagnetic Compability

RMA - Return Material Authorization

PCI - Peripheral Component Interconnect

USB - Universal Serial Bus

RTC - Real Time Clock

SPI - Serial Peripheral Interface

USART - Universal Synchronous/Asynchrnonous Receiver/Transmitter

FPGA - Field Programmable Gate Array

PHY - Ethernet physical layer

MAC - Ethernet medium access control

UTP - Unshielded Twisted Pair

MDIO - Management Data Input/Output (IEEE 802.3)

MII - Media Independent Interface

RMII - Reduce Media Independent Interface

FIFO - First in First out data buffer

CRC - Cyclic Redundancy Check

ADC - Analogue to Digital converter

DAC - Digital to Analogue converter

LCD - Liquid Crystal Display

CAN - Controller Area Network (field-bus often used in vehicles)

SDRAM - Synchronous Dynamic Random Access Memory

Appendix G Product care and maintenance

The H6042 is a "naked board" aim to be embedded in a product and casing. Therefore the board is sensitive for ESD and should be handled in ESD safe environment. At least utilize a wrist-strap when handled, but preferably handle the board in a ESD-safe lab or production area.

When the board is mounted on a carrier board make shore the boards signalground is at the same potential. This may be reach safely by connecting the signal ground of the boards to a common GND, with a series resistor.

Always remember to power off the system when assembling and disassembling.

Appendix H RMA - Return Material Authorization

In case of a malfunction unit, the following RMA procedure is to be used.

Contact Hectronic support department at support@hectronic.se. The support department will guide you through the RMA process.

Appendix I Hectronic ARM board family summary

Article	Description
H6042	ARM board with a Spartan FPGA as a companion chip
H4090	Reference carrier for H6042
H6043	Very small ARM board
H4091A	Carrier board for H6043, equipped with Ethernet PHY and USB and a +5V step-up converter
H4091B	Debug connector board for H6043.
H4091C	Button board for connection to H4091A
H4091D	RFID board, for connection to H4091A

Table 21: Hectronic ARM products.