



H4090 Manual

Electrical and mechanical specifications of the H4090 carrier board

Title:	H4090 Manual
Subject:	Electrical and mechanical specifications of the H4090 carrier board
Document number:	D0005
Version:	1.3
Last updated:	2/20/09

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1 Document Information

1.1 Abstract

This document describes the pinout and mechanics for Hectronic H4090, a H6042 carrier board.

1.2 Document revisions

Rev.	Date	Sign	Description
1.0	2007-08-02	Daniel Skaborn	Initial release
1.1	2008-03-17	Jonas Antoni	Extracted H4090 information to a separate manual
1.2	2008-05-28	Jonas Antoni	Pin J13.24 has changed between R1.0 and R1.1
1.3	2009-01-09	Jonas Antoni	Fixed J8.50 to be "PCI AD01". Fixed J8.28 to be "PCI CBE1-". Fixed markings in drawing indication pin 1 on connectors.

Table 1: Document revisions.

1.3 References

No.	Description
[1]	H6042 Manual
[2]	http://www.atmel.com/dyn/resources/prod_documents/doc1768.pdf


Table 2: Document references.

2 Safety Instructions



Electrostatic discharge (ESD) damage can result in partial or complete device failure, performance degradation, or reduced operation life. To avoid ESD damage, the following precautions are strongly recommended.

- Keep the board in its ESD shielding bag until you are ready to install it.
- Before touching the board, attach an ESD wrist strap to your wrist and connect its other end to a known ground.
- Handle the device only in an area that has its working surfaces, floor coverings, and chairs connected to a known ground.
- Hold the device only by its edges and mounting hardware. Avoid touching components and connector pins.
- Please assure ESD compliant handling of the board when unpacking and connecting peripherals.
- Never connect or disconnect external peripherals with power on.

- Please study all the information in this document carefully before applying power to the system.
- For further information on ESD, visit www.esda.org .

3 Product overview

3.1 Module layout

Key components and connector functions.

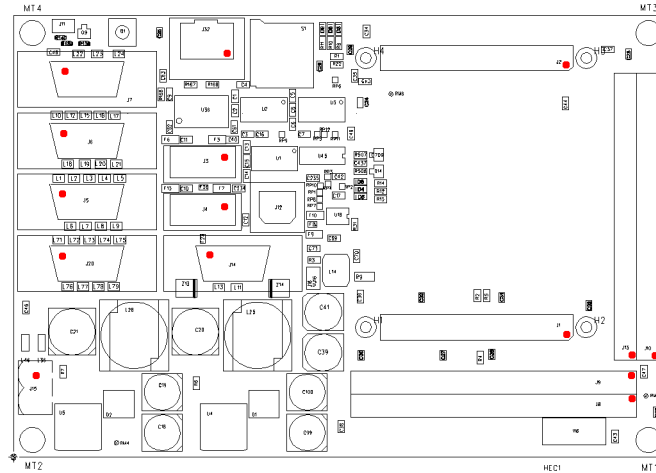


Figure 1: Connectors and components, top view

3.2 Models and options

Model	Description
H4090-01	A H4090 with all options mounted except the PCI connector mounted.

Table 3: H4090 CCOs/Models

4 Product specifications

4.1 Mechanical

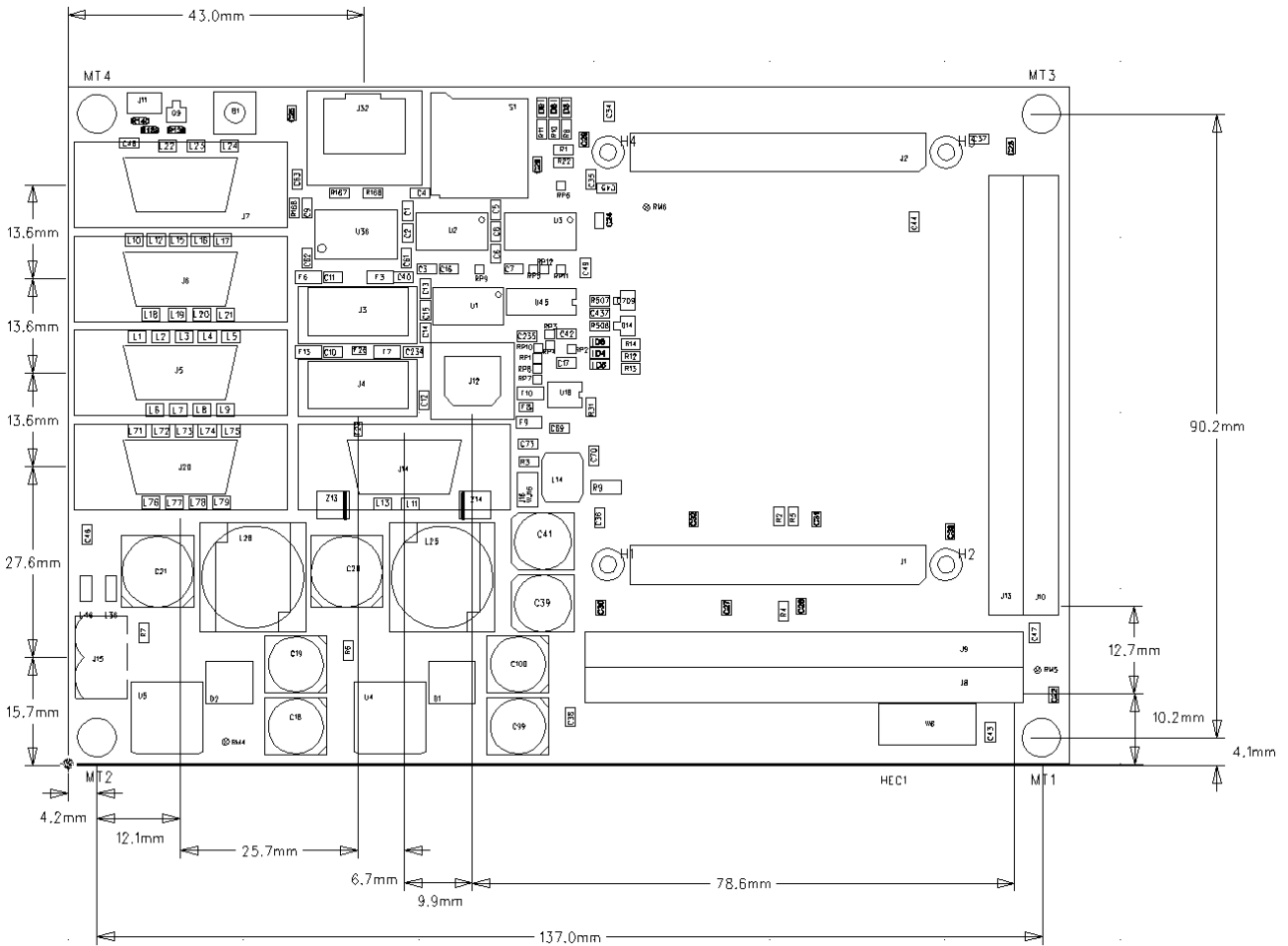


Figure 2: Mechanical drawing, top side view

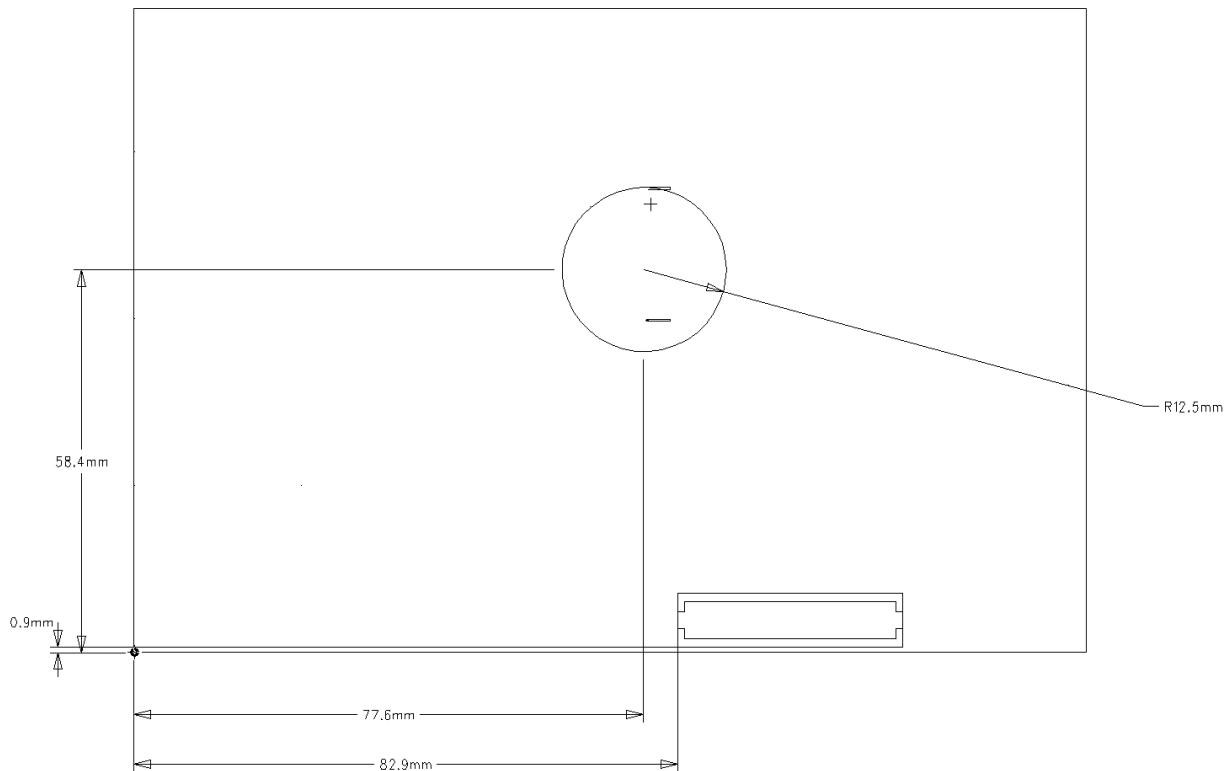


Figure 3: Mechanical drawing, bottom side view

4.1.1 Component heights

The maximum component height on the top side is 16 mm, and 5 mm on the bottom side. If the optional PCI connector (P7) is mounted the maximum component height on the bottom side is extended to 11 mm.

There are no additional restrictions than those stated for the mounted CPU board, see the manual for the CPU board.

4.1.2 Assembly of a CPU board and H4090

The connectors connecting the H4090 with its CPU board are fragile. When inserting or removing a CPU board from the H4090 the same amount of force must be applied to both board-to-board connectors at the same time.

If the force used to insert/remove the CPU board isn't applied straight from above the board-to-board connectors may break.

4.2 Electrical

4.2.1 Power supply requirements

The H4090 requires the power supply sources to be within voltage ranges to work properly.

Supply	Min	Max	Unit
--------	-----	-----	------

VCC 12 V	9	15	V
----------	---	----	---

Table 4: Power supply.

4.2.2 Power consumption

The following values are calculated estimations. (The actual unit may consume more.)

Module mounted	Max dissipation at 12V ¹	Typical dissipation at 12V	Unit
H4090 only	580	30	mA
H6042 with a Spartan3E250	TBD ²	TBD ²	mA
H6042 with a Spartan3E500	700 mA	150 mA	mA
H6042 with a Spartan3E1200	TBD ²	TBD ²	mA

Table 5: Power consumption.

¹The maximum dissipation numbers includes two USB device loads of 0.5 A / each.

²Not measured yet due to shortage of fabricated units.

4.3 Thermal

In operating areas where the board is surrounded by air there is no need for nor active cooling or passive heat sink.

5 Board description

5.1 Block diagram

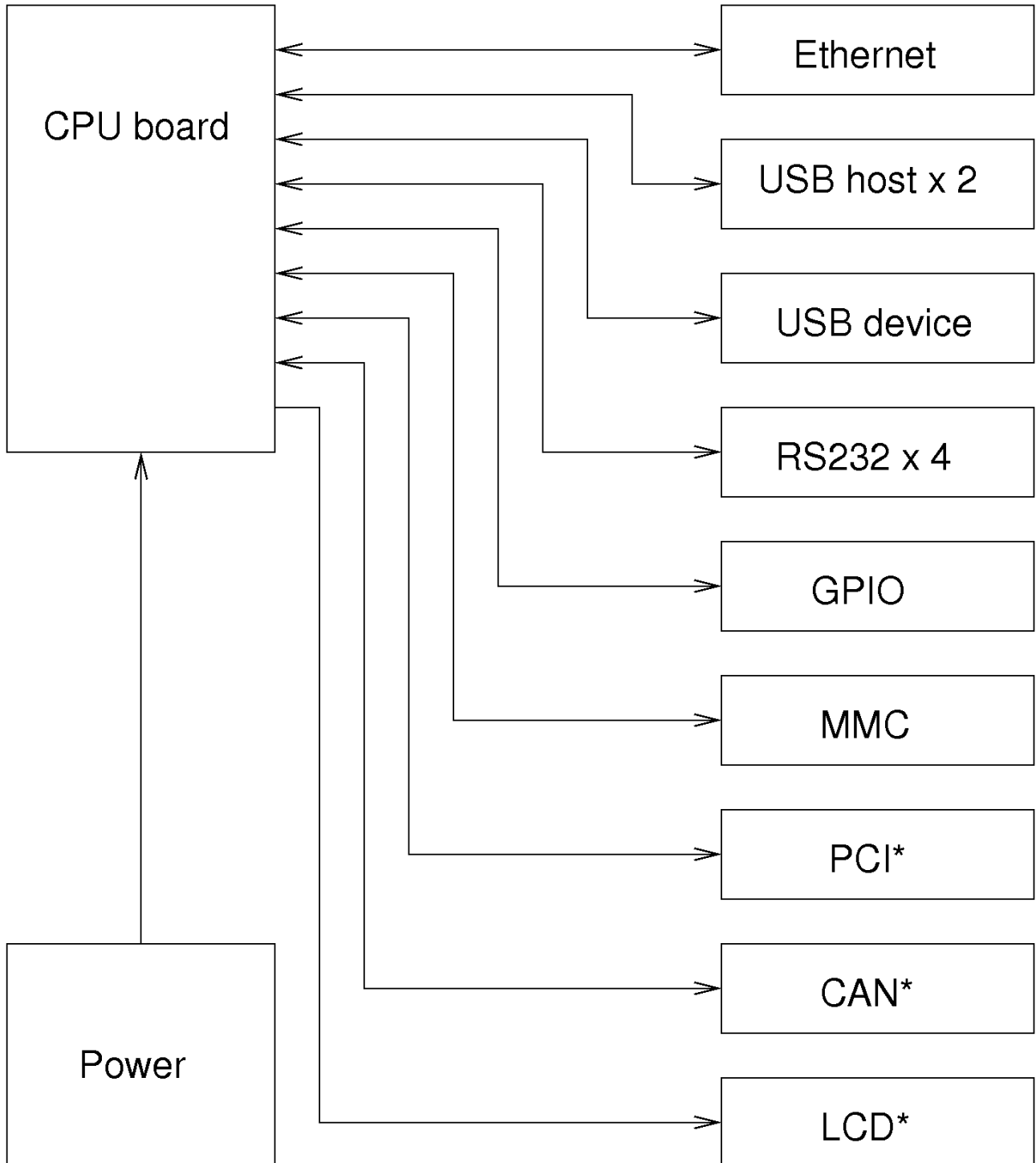


Figure 4: Block diagram over the H4090

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*Only supported if implemented on CPU board.

5.2 Ethernet

The H4090 adds necessary Ethernet magnetics and a standard RJ45 connector for network communication.

5.3 USB host

The H4090 has support for two USB host connections with +5 V power supply to the devices.

5.4 USB device

The H4090 has one USB device port. The H4090 can't be powered by the USB host, it must have it's own power source.

5.5 RS232

The H4090 has support for four RS232 channels. One of these are usually used for debugging purposes, and the rest for applications.

5.6 GPIO

The GPIO available at the I/O headers (J8, J9, J10 and J13) are connected directly to the ARM CPU and/or the FPGA and uses +3.3 V logical levels.



Maximum voltage that may be applied to these pins are 3.6V.

On the GPIO pins many other interfaces are available as well, such as SPI and I2C. See the Atmel AT92RM9200 manual and the H6042 manual.

5.7 MMC

There is a connector for MMC on the H4090 which is connected to the SPI bus on the CPU board.

5.8 PCI bus

The use of the PCI bus requires that the CPU board supports PCI. By default this is NOT included in the H6042.

Contact Hectronic for further information.

5.9 LCD interface

The use of the LCD interface requires that the CPU board supports LCD. By default this is NOT included in the H6042.

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Contact Hectronic for further information.

5.10 CAN bus

The use of the CAN bus requires that the CPU board supports CAN. By default this is NOT included in the H6042.

Contact Hectronic for further information.

6 Quality and environmental data

6.1 Required environmental conditions

Temperature ambient, operating	-40 to +80 °C
Temperature ambient, storage	-40 to +80 °C

Table 6: Environmental conditions.

6.2 EMC compliance

When correctly installed in a suitable chassis with recommended filtering on carrier-board as described in the design guidelines, the H4090 is designed to meet the following EMC regulations.

EN50081-1 Generic emission standard for residential commercial and light industry use.

CISPR25 RF-disturbances for vehicles (e-type approval).

6.3 Safety compliance

Depending on carrier board design, and mechanic casing.

6.4 Industry standard compliances

The H4090 implements the following industry standards. To fulfil the standards some filtering/drivers are needed on the carrier board.

Standard	Description	Reference
USB 2.0	Universal Serial Bus rev 2.0	http://www.usb.org
IEEE 802.3i	Ethernet 10Base-T	http://www.ieee.org
IEEE 802.3u	Fast Ethernet 100Base-Tx	http://www.ieee.org
I2C	Inter-Integrated Circuit bus	NXP (formerly Philips) I ² C 2.1 specification (January 2000)
SPI	Serial Peripheral Interface BUS	No formal spec. exists. First introduced by Freescale (formerly Motorola)
RS232	Serial communication standards	ANSI / TIA / EIA and the international equivalent from ITU

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IEEE 1149.1	JTAG Boundary Scan (ARM CPU)	http://www.ieee.org 

6.5 Quality ensures and milieu influences

RoHS compliant

ISO9001

ISO14001

6.5.1 WEEE 2002/96/EC

The H4090 is intended to be included in a product. The responsibility when it comes to recycling and registering the end product with the correct authorities lies at the producer of the end product.

Appendix A Connectors and pinouts

A.1 Connector placements

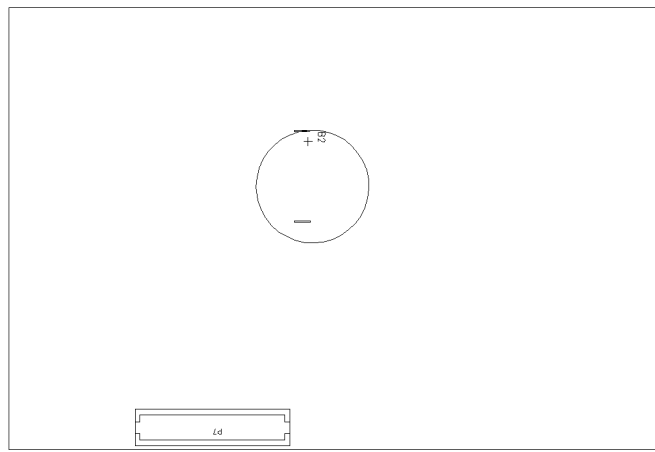


Figure 5: Connectors and components, bottom view

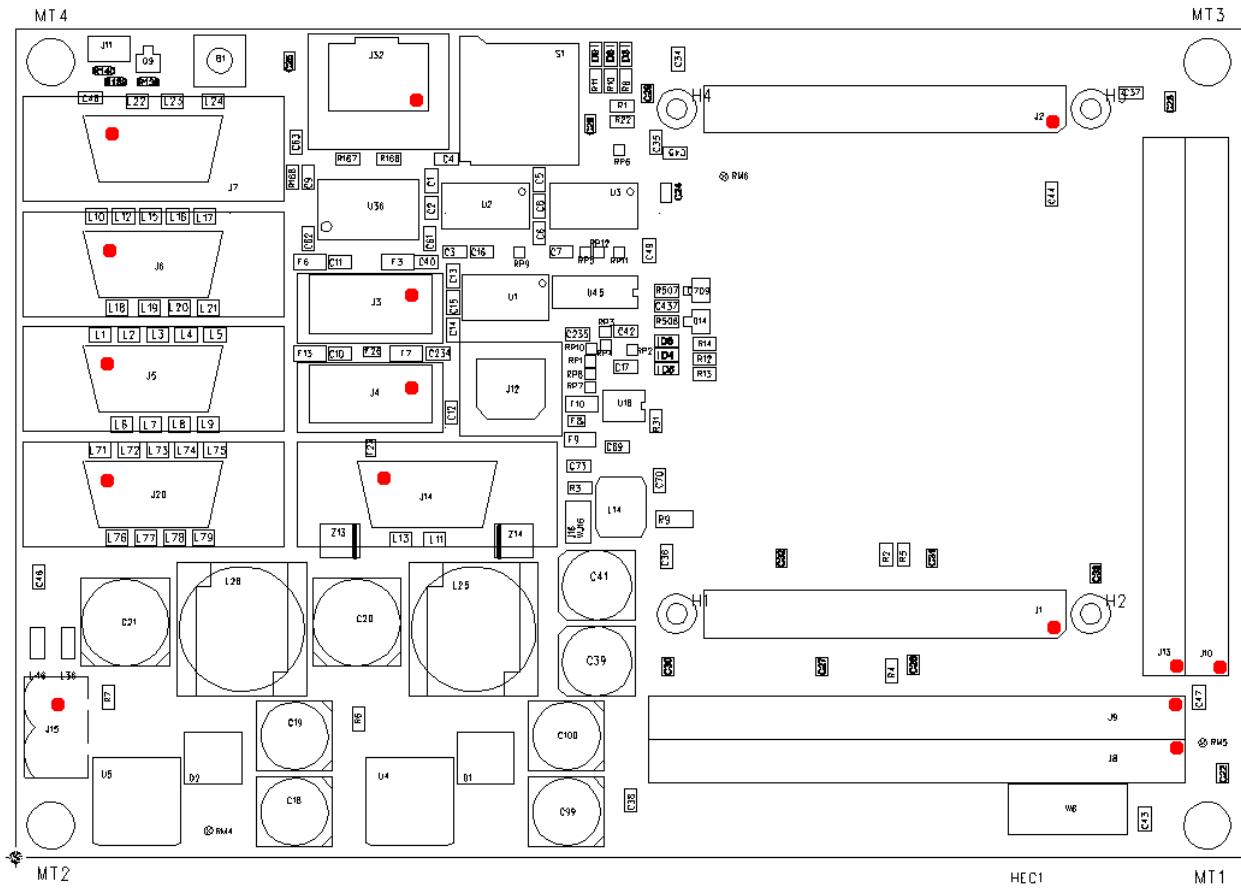


Figure 6: Connectors and components, top view

Pin #1 is above indicated by a red dot, on the PCB pin #1 may be identified by it's square pad.

A.2 J7 - RS232 Serial Debug port 9pol DSUB

This is the debug port where the initial console will appear. Connect it to the host with a straight cable

pin#	signal	class
1		
2	TX	rs232
3	RX	rs232
4		
5	GND	
6		
7		
8		
9		

Table 7: J7 pinout.

A.3 J6 - RS232 Serial port 9pol DSUB

This serial port is connected to USART2 on the ARM CPU

pin#	signal	class
1	DCD	rs232
2	RX	rs232
3	TX	rs232
4	DTR	rs232
5	GND	
6	DSR	rs232
7	RTS ¹	rs232
8	CTS ¹	rs232
9	RI	rs232

Table 8: J6 pinout.

¹Note that RTS/CTS for USART2 are shared with the RX/TX on the debug port ([J7](#)).

A.4 J5 - RS232 Serial port 9pol DSUB

This serial port is connected to USART1 on the ARM CPU

pin#	signal	class
1	DCD	rs232
2	RX	rs232
3	TX	rs232
4	DTR	rs232
5	GND	
6	DSR	rs232
7	RTS	rs232
8	CTS	rs232
9	RI	rs232

Table 9: J5 pinout

A.5 J20 - RS232 Serial port 9pol DSUB

This serial port is connected to USART0 on the ARM CPU

pin#	signal	class
1	DCD	rs232
2	RX	rs232
3	TX	rs232
4	DTR	rs232
5	GND	
6	DSR	rs232

7	RTS	rs232
8	CTS	rs232
9	RI	rs232

Table 10: J20 pinout

A.6 J14 - CAN port 9pol DSUB

Optional, not mounted by default.

See note about [CAN](#) FPGA firmware.

pin#	signal	class
1		
2	CAN LOW	can
3	GND	
4		
5	GND	
6	GND	
7	CAN HIGH	can
8		
9	+5V (OUT CURRENT LIM)	pow5

Table 11: J14 pinout

A.7 J32 - 100Mbit Ethernet

Standard RJ45 jack for Ethernet

pin#	signal	class
1	TX+	eth
2	TX-	eth
3	RX+	eth
4		
5		
6	RX-	eth
7		
8		

Table 12: J32 pinout

A.8 J3 - USB1 host

Standard USB host connector.

pin#	signal	class
1	+5V	usbo
2	D-	usbd

3	D+	usbd
4	GND	

Table 13: J3 pinout

A.9 J4 - USB0 host

Standard USB host connector.

pin#	signal	class
1	+5V	usbo
2	D-	usbd
3	D+	usbd
4	GND	

Table 14: J4 pinout

A.10 J12 - USB device

Standard USB device connector.

pin#	signal	class
1	+5V (detect)	usbp
2	D-	usbd
3	D+	usbd
4	GND	

Table 15: J12 pinout

A.11 J8 - IO header

pin#	signal	class
1	+3.3V	pow33
2	GND	
3	ARM PB29	alog
4		
5	ARM PB28	alog
6	GND	
7	ARM PA2	alog
8	ARM PA1	alog
9	ARM PA0	alog
10	ARM PA3	alog
11	ARM PA4	alog
12	GND	
13	PCI CLK0	slog
14		

15	PCI REQ0-	slog
16	GND	
17	PCI AD31	slog
18	PCI AD29	slog
19	PCI AD27	slog
20	PCI AD25	slog
21		
22	PCI CBE3-	slog
23	PCI AD23	slog
24	GND	
25	PCI AD21	slog
26	PCI AD19	slog
27	PCI AD17	slog
28	GND	
29	PCI CBE2	slog
30	PCI IRDY-	slog
31		
32	PCI DEVSEL-	slog
33		
34	GND	
35	PCI PERR-	slog
36	PCI SERR-	slog
37		
38	PCI CBE1-	slog
39	PCI AD14	slog
40	GND	
41	PCI AD12	slog
42	PCI AD10	slog
43	GND	
44	PCI AD08	slog
45	PCI AD07	slog
46		
47	PCI AD05	slog
48	PCI AD03	slog
49	GND	
50	PCI AD01	slog

Table 16: J8 pinout

A.12 J9 - IO header

pin#	signal	class
------	--------	-------

1	FPGA GENERIC1	slog
2	FPGA GENERIC2	slog
3	FPGA CANRX	slog
4	FPGA CANTX	slog
5	GND	
6	ARM PD10	alog
7	ARM PD9	alog
8	ARM PD8	alog
9	ARM PD7	alog
10	GND	
11	PCI INT A-	slog
12	GND	
13	PCI RST-	slog
14	PCI GNT0-	slog
15	PCI PME-	slog
16		
17	PCI AD30	slog
18	GND	
19	PCI AD28	slog
20	PCI AD26	slog
21		
22	PCI AD24	slog
23		
24	GND	
25	PCI AD22	slog
26	PCI AD20	slog
27		
28	PCI AD18	slog
29	PCI AD16	slog
30	GND	
31	PCI FRAME-	slog
32	GND	
33	PCI TRDY-	slog
34		
35	PCI STOP-	slog
36	GND	
37	PCI PAR	slog
38	PCI AD15	slog
39		
40	PCI AD13	slog
41	PCI AD11	slog

42	GND	
43	PCI AD09	slog
44	PCI CBE0-	slog
45		
46	PCI AD06	slog
47	PCI AD04	slog
48	GND	
49	PCI AD02	slog
50	PCI AD00	slog

Table 17: J9 pinout

A.13 J10 - IO header

pin#	signal	class
1	LCD D0	slog
2	LCD D1	slog
3	GND	
4	LCD D2	slog
5	LCD D3	slog
6	GND	
7	LCD D4	slog
8	LCD D5	slog
9	GND	
10	LCD D6	slog
11	LCD D7	slog
12	GND	
13	LCD D8	slog
14	LCD D9	slog
15	GND	
16	LCD D10	slog
17	LCD D11	slog
18	GND	
19	LCD D12	slog
20	LCD D13	slog
21	GND	
22	LCD D14	slog
23	LCD D15	slog
24	GND	
25	LCD D16	slog
26	LCD D17	slog
27	GND	

28	LCD SYNC	slog
29	LCD HSYNC	slog
30	LCD DEN	slog
31	LCD CC	slog
32	GND	
33	LCD DOTCLK	slog
34	+5V	pow5
35	+5V	pow5
36	+5V	pow5
37	GND	
38	USART CTS TTL	alog
39	USART RTS TTL	alog
40	USART RX TTL	alog
41	USART TX TTL	alog
42	ARM PB2	alog
43	ARM PA24	alog
44	ARM PB22	alog
45	ARM PA19	alog
46	GND	
47	ARM PA31	alog
48	TWD	alog
49	TWCK	alog
50	ARM PC6 R	alog

Table 18: J10 pinout

A.14 J13 - IO header

pin#	signal	class
1	ARM PB5	alog
2	ARM PB6	alog
3	ARM PB7	alog
4	ARM PB8	alog
5	GND	
6	ARM PB9	alog
7	ARM PB10	alog
8	ARM PB11	alog
9	ARM PB12	alog
10	GND	
11	ARM PB13	alog
12	ARM PB14	alog
13	ARM PB15	alog

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14	ARM PB16	alog
15	ARM PB17	alog
16	+3.3V	pow33
17	GND	
18	ARM PA27	alog
19	ARM PA28	alog
20	ARM PA29	alog
21	+3.3V	pow33
22	ARM PB3	alog
23	ARM PA4	alog
24	Up to H4090R10: ARM PB5 From H4090R11: CAN_OVERCUR	alog
25	+3.3V	pow33
26	ARM PB4	alog
27	GND	
28	EXTERNAL RESET IN	rst
29	POWERGOOD PS	pgd
30	POWERGOOD LP3982	pgd
31	GND	
32	ARM JTAG TMS	alog
33	ARM JTAG TDI	alog
34	ARM JTAG TDO	alog
35	ARM JTAG TCK	alog
36	GND	
37	+3.3V	pow33
38	FPGA JTAG TMS	slog
39	FPGA JTAG TDI	slog
40	FPGA JTAG TDO	slog
41	FPGA JTAG TCK	slog
42	GND	
43		
44		
45	GND	
46	ETH1 LINKSTATUS	ethl
47	ETH1 LINK/ACTIVE-	ethl
48	ETH1 DUPLEX	ethl
49	+3.0V BAT	bat
50	+3.3V ETH	pow33

Table 19: J13 pinout

A.15 P7 - PCI expansion header

Optional, not mounted by default.

See note about [PCI](#) FPGA firmware.

pin#	signal	class
A1		
A2		
A3	GND	
A4		
A5	GND	
A6	GND	
A7		
A8	GND	
A9	PCI AD29	slog
A10	PCI AD25	slog
A11	PCI CBE3-	slog
A12	GND	
A13	PCI AD19	slog
A14	GND	
A15	PCI IRDY-	slog
A16	PCI DEVSEL-	slog
A17	GND	
A18	PCI SERR-	slog
A19	PCI CBE1-	slog
A20	GND	
A21	PCI AD10	slog
A22	PCI AD08	slog
A23		
A24	PCI AD03	slog
A25	PCI AD01	slog
B1		
B2		
B3		
B4		
B5		
B6	PCI CLK0	slog
B7	PCI REQ0-	slog
B8	PCI AD31	slog
B9	PCI AD27	slog
B10		
B11	PCI AD23	slog
B12	PCI AD21	slog

B13	PCI AD17	slog
B14	PCI CBE2-	slog
B15		
B16		
B17	PCI PERR-	slog
B18		
B19	PCI AD14	slog
B20	PCI AD12	slog
B21	GND	
B22	PCI AD07	slog
B23	PCI AD05	slog
B24	GND	
B25		
C1		
C2	GND	
C3		
C4	GND	
C5		
C6	GND	
C7	PCI GNT0-	slog
C8		
C9	GND	
C10	PCI AD26	slog
C11	PCI AD24	slog
C12	GND	
C13	PCI AD20	slog
C14	PCI AD18	slog
C15	GND	
C16	GND	
C17		
C18	GND	
C19	PCI AD15	slog
C20	PCI AD13	slog
C21	GND	
C22	PCI CBE0-	slog
C23	PCI AD06	slog
C24	GND	
C25	PCI AD00	slog
D1	PCI INTA-	slog
D2		
D3		

D4		
D5		
D6	PCI RST-	slog
D7	PCI PME-	slog
D8	PCI AD30	slog
D9	PCI AD28	slog
D10		
D11		
D12	PCI AD22	slog
D13		
D14	PCI AD16	slog
D15	PCI FRAME-	slog
D16	PCI TRDY-	slog
D17	PCI STOP-	slog
D18	PCI PAR	slog
D19		
D20	PCI AD11	slog
D21	PCI AD09	slog
D22		
D23	PCI AD04	slog
D24	PCI AD02	slog
D25		

Table 20: P7 pinout

A.16 J15 - Power input

pin#	signal	class
1	+12 V (9-15V)	pow
2	GND	

Table 21: J15 pinout

A.17 S1 - MMC expansion slot

pin#	H4090r10/r11	H4090r12	class
1	-	DAT2/ARM PB4	
2	CS/ARM PA3	DAT3/ARM PB5	alog
3	DI/ARM PA1	CMD/ARM PA28	alog
4	VDD	VDD	pow33
5	SCLK/ARM PA2	CLK/ARM PA27	alog
6	GND	GND	
7	DO/ARM PA0	DAT0/ARM PA29	alog

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8	-	DAT1/ARM PB3	alog

Table 22: S1 pinout

Appendix B Signal characteristics

Each signal in the pin signal listings have a class tag. Here follows descriptions of the different signal classes on the board.

B.1 pow - power line

This is a power supply (input) connection.

B.2 pow33 - +3.3 V

+3.3 V generated by the H4090.

B.3 pow5 - +5 V

+5 V generated by the H4090.

B.4 eth - Ethernet data signal

The Ethernet signals are differential pair signal. Length matching and differential impedance are critical parameters. A line transformer is needed before connecting to standard Ethernet cabling.

B.5 ethl - Ethernet LED status signal

These are the signals for status LEDs. Current limiting series resistors must be used.

B.6 alog - ARM CPU logic level signal

ARM CPU logic level signal. Pins has a programmable pull-up resistor of 15kOhm. After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that must be enabled as peripherals at reset. Signals is 3.3V logic level.



Maximum voltage that may be applied to these pins are 3.6V.

B.7 slog - Spartan 3E FPGA logic level signal

Spartan FPGA logic level signal. Depending on the FPGA firmware, the pins can either be input or output. Signals are 3.3V logic level.



Maximum voltage that may be applied to these pins are 4.3V.

B.8 rs232 - RS232 signals

Input/output signals according to the RS-232 standard.

B.9 can - CAN signals

Differential signals according to the CAN standard.

B.10 rst - Reset input signal

External reset signal, pulse to ground to achieve a system reset. Signal should be high-impedance or open to let system run.

B.11 usbd - USB data signal

The USB signals are differential pairs. Length matching, maximum length and differential impedance are critical design parameters. The pairs should be common mode filtered before cable connector to avoid conductive EMC problems.

B.12 usbp - USB device power input

The USB device power input signal is only used for detection of a connected host controller. A host controller should supply this pin with its 5V pin.

B.13 usbo - USB device power output

USB host power output. +5V generated by the H4090.

B.14 pgd - Power good

Output signal which is asserted high when the power on the CPU board is considered stable.

Appendix C Notational conventions and acronyms used

C.1 Notational conventions

All numbers are decimal unless otherwise stated.

Bit 0 is the low-order bit.

If a bit is set to 1, the associated description is true unless otherwise stated.

C.2 Acronyms

ESD - Electro Static Discharge

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- EMC - ElectroMagnetic Compability
- RMA - Return Material Authorization
- PCI - Peripheral Component Interconnect
- USB - Universal Serial Bus
- RTC - Real Time Clock
- SPI - Serial Peripheral Interface
- USART - Universal Synchronous/Asynchronous Receiver/Transmitter
- FPGA - Field Programmable Gate Array
- PHY - Ethernet physical layer
- MAC - Ethernet medium access control
- UTP - Unshielded Twisted Pair
- MDIO - Management Data Input/Output (IEEE 802.3)
- MII - Media Independent Interface
- RMII - Reduce Media Independent Interface
- FIFO - First in First out data buffer
- CRC - Cyclic Redundancy Check
- ADC - Analogue to Digital converter
- DAC - Digital to Analogue converter
- LCD - Liquid Crystal Display
- CAN - Controller Area Network (field-bus often used in vehicles)
- SDRAM - Synchronous Dynamic Random Access Memory

Appendix D Product care and maintenance

The H4090 is a "naked board" aim to be embedded in a product and casing. Therefore the board is sensitive for ESD and should be handled in ESD safe environment. At least utilize a wrist-strap when handled, but preferably handle the board in a ESD-safe lab or production area.

When the board is mounted on a carrier board make shore the boards signalground is at the same potential. This may be reach safely by connecting the signal ground of the boards to a common GND, with a series resistor.

Always remember to power off the system when assembling and disassembling.

Appendix E RMA - Return Material Authorization

In case of a malfunction unit, the following RMA procedure is to be used.

Contact Hectronic support department at support@hectronic.se. The support department will guide you through the RMA process.

Appendix F Hectronic ARM board family summary

Article	Description
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Title		Document no	
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H6042	ARM board with a Spartan FPGA as a companion chip
H4090	Reference carrier for H6042
H6043	Very small ARM board
H4091A	Carrier board for H6043, equipped with Ethernet PHY and USB and a +5V step-up converter
H4091B	Debug connector board for H6043.
H4091C	Button board for connection to H4091A
H4091D	RFID board, for connection to H4091A

Table 23: Hectronic ARM products.